#### HOW TO DEVELOP WITH NTAG 5 NTAG 5 WEBINAR SERIES

PABLO FUENTES FEBRUARY 2020





SECURE CONNECTIONS FOR A SMARTER WORLD

PUBLIC



## Agenda

- NTAG 5 Family Overview
- General development considerations
- Using GPIO features
- Using PWM features
- Using Pass-through mode
- Using I<sup>2</sup>C master mode
- More support



# **NTAG 5 Family Overview**



### **NTAG 5 Family Overview Positioning**





## **NTAG 5 Family**

	NTAG 5 switch	<ul> <li>Control and dim LEDs</li> <li>Calibrate reference current without MCU</li> <li>Verify authenticity of the device</li> </ul>	
(	NTAG 5 link	<ul> <li>Draw power from the NFC reader to supply sensors</li> <li>Read out sensor information without an MCU*</li> <li>Secure sensor interaction</li> </ul>	SRAM     I <sup>2</sup> C       EEPROM     I 0 1 0 1 0       TRANSPARENT IPC MASTER CHANNEL     e.g       T sonsor
(	NTAG 5 boost	<ul> <li>Smallest footprint antenna</li> <li>Enables NTAG 5 link features for tiny solutions</li> </ul>	ALM SRAM EEPROM TRANSPARENT IPC MASTER CHANNEL P.g T sensor
4	Training Mobile . Knowledge		



### **NTAG 5 Family Overview Development kits**

NTAG 5 link Evaluation board (OM23510ARD)

- Integrating NTAG 5 link (NTP5332) •
- 54 x 27 mm Plutus antenna •
- Jumper to select between different supply voltages •
- Hard-power-down button •
- Arduino header .
- Easy to access wired interface signals through pins .





NTAG 5 boost Evaluation board (OM23511ARD)

- Integrating NTAG 5 boost (NTA5332)
- 10 x 10 mm Active antenna •
- Jumper to select between different supply voltages •
- Hard-power-down button
- Arduino header
- Easy to access wired interface signals through pins





General development considerations



### General development considerations Content

- Main supported commands (NFC interface)
- Configuring NTAG 5 wired interface
- Setup used for examples







### General development considerations Main commands supported (NFC interface)

WRITE\_CONFIG (Command code C1h) Command WRITE\_CONFIG UID (optional) CRC16 Manuf. Code **Block Address** Flags Data 8 bits 8 bits 8 bits 64 bits 8 bits 32 bits 16 bits Response Error Code 8 bits / 16 bits

#### READ\_CONFIG (Command code COh)

Flags	READ_CONFIG	Manuf. Code	UID (optional)	Block Address	N° of blocks	CRC16	Command
8 bits	8 bits	8 bits	64 bits	8 bits	8 bits	16 bits	

Response	Flags	Data	CRC16
	8 bits	N° of block x 32 bits	16 bits

For Read Single Block and Write Single Block (EEPROM access) refer to ISO15693 or NFC Forum Type 5 tag specifications



For more information on Flags and Error code refer to ISO15693 specifications



### General development considerations Configuring wired interface

NTAG 5 wire interface must be configured depending on the application. It can be configured via:

- NFC Interface (Recommended)
  - Always configurable through NFC interface
- I<sup>2</sup>C Interface
  - Only available if preconfigured as I<sup>2</sup>C Slave
  - Configuration not reversible through I<sup>2</sup>C interface

 $^{\ast}$  I²C interface not supported in NTAG 5 switch version

\*\* I<sup>2</sup>C master only supported in NTP5332 and NTA5332





#### General development considerations Configuring wired interface

• Wired interface is configured through USE\_CASE\_CONF parameter from Configuration bytes block.

Most of the wired interface registers have both configuration and session registers.

#### Session registers:

- ✓ Changes take effect immediately
- X Not persistent after reset

#### Configuration settings:

- ✓ Value remains valid after chip reset.
- x No immediate effect



Block A	Address	Bvte 0	Bvte 1	Bvte 2	Bvte 3		
NFC	I <sup>2</sup> C				29:00		
37h	37h 1037h A1h 10A1h				DELL		
A1h			CONFIG_1	CONFIG_Z	RFU		

Bit	Name	Value	Description						
7		0b	ARBITER_MODE needs to be set after startup						
/	EH_ARBITER_WODE_EN	1b	ARBITER_MODE is set automatically in any case after startup						
4		0b	PLM						
0		1b	ALM mode when supplied by Vcc else PLM (default)						
		00b	I <sup>2</sup> C slave (default)						
	USE_CASE_CONF	01b	I <sup>2</sup> C master						
4-5		10b	GPIO / PWM						
		11b	All host interface functionality disabled						
	ARBITER_MODE	00b	Normal mode (default)						
2.2		01b	SRAM mirror mode						
2-3		10b	SRAM pass-through mode						
		11b	SRAM PHDC mode						
1		0b	SRAM not accessible (default)						
I	SKAWI_ENADLE	1b	SRAM is available (when Vcc supplied)						
0		0b	Data transfer direction is I <sup>2</sup> C to NFC (default)						
0		1b	Data transfer direction is NFC to I <sup>2</sup> C						

#### Session register address

#### General development considerations Setup used for examples

#### NTAG 5 link evaluation board



#### KW41Z development board (FRDM-KW41Z)

- NXP's ultra-low-power KW41Z Wireless MCU
- Fully compliant Bluetooth v4.2 Low Energy
- 4-Mbit external serial flash memory for OTAP support
- Two LED indicator (One RGB and one red)
- Two push-button switches
- Two TSI buttons
- Arduino compatible header



11 🚺

# **Using GPIO features**



#### General development considerations Configuring wired interface

- NEC
- Wired interface is configured through USE\_CASE\_CONF parameter from Configuration bytes block.

Most of the wired interface registers have both configuration and session registers.

#### Session registers:

- ✓ Changes take effect immediately
- X Not persistent after reset

#### Configuration settings:

- ✓ Value remains valid after chip reset.
- X No immediate effect



E	Block Address			Byte 0		Byte 1		Byte 2	Byte 3
NFC	;	I <sup>2</sup> C		Dyteo		Dyter		Dyte 2	Dyte 5
37h	۱	1037h				CONFIC 1			DELL
A1h	۱	10A1h		CON	CONFIG_0	CONTIN	10_1	CONFIG_2	KFU
Name Value			lue			l	Description		

Session register address

Bit	Name	Value	Description					
7		0b	ARBITER_MODE needs to be set after startup					
7	EH_ARBITER_MODE_EN	1b	ARBITER_MODE is set automatically in any case after startup					
6		0b	PLM					
		1b	ALM mode when supplied by Vcc else PLM (default)					
4-5		00b	I <sup>2</sup> C slave (default)					
	USE_CASE_CONF	01b	I <sup>2</sup> C master					
		10b	GPIO / PWM					
		11b	All host interface functionality disabled					
	ARBITER_MODE	00b	Normal mode (default)					
2.2		01b	SRAM mirror mode					
2-3		10b	SRAM pass-through mode					
		11b	SRAM PHDC mode					
1		0b	SRAM not accessible (default)					
I	SKAWI_ENADLE	1b	SRAM is available (when Vcc supplied)					
0		0b	Data transfer direction is I <sup>2</sup> C to NFC (default)					
0		1b	Data transfer direction is NFC to I <sup>2</sup> C					

### Using GPIO features Configuring wired interface

#### Step 2

- Define if pads are used as GPIO or PWM
- For GPIO pads, we should also define if they are destined as output or input pads

Wired interface registers have both configuration and session registers.

Session registers:

- ✓ Changes take effect immediately
- X Not persistent after reset

Configuration settings:

- ✓ Value remains valid after chip reset.
- X No immediate effect



							Session	register ad	ddres
		Block A	Address	Ву	/te 0	Byte 1	Byte 2	Byte 3	
		39h 1039h PWM		_GPIO_	PWM_GPIO_				
		A3h	10A3h	CONFI	G_0_REG	CONFIG_1_REG		0	
В	Bit Name			Value	Desc	cription			
	7 GPIO1_SDA_PAD_OUT_STATUS			STATUS	0b	Output status on pad is	LOW		
				STATUS	1b	Output status on pad is HIGH			
	6 GPIOD SCL PAD OUT STATUS			STATUS	0b	Output status on pad is LOW			
	GPIOU_SCL_PAD_OUT_STATUS		517(105	1b	Output status on pad is HIGH				
,	5	GPI01	SDA PAD IN S	τατμς	0b	Input status			
	0				1b				
	4	GPIO0	SCL PAD IN S	TATUS	0b	Innut status			
					1b	input status			
	3		GPIO1 SDA PAD	)	0b	Output			
	-				1b	Input			
	2		GPIO0 SCL PAD		0b	Output			
					1b	Input			
	1	GPI	01_PWM1_SDA_	PAD	0b	GPIO			
					1b	PWM			
(	0	GPI	00_PWM0_SCL_	PAD	0b	GPIO			
		GPIOU_PWMU_SCL_P			1b	PWM			

### Using GPIO features Changing GPIO line state (output)

#### Setting up line state

Write to PWM\_GPIO\_CONFIG\_REG on bit 6 or bit 7 depending on the line chosen

- Write 0b to set line to LOW state
- Write 1b to set line to HIGH state

Wired interface registers have both configuration and session registers.

#### Session registers:

- ✓ Changes take effect immediately
- X Not persistent after reset

Configuration settings:

- ✓ Value remains valid after chip reset.
- X No immediate effect





### Using GPIO features Reading GPIO line state (input)

#### Monitoring line state

Read STATUS1\_REG bit 3 or bit 4 depending on the line chosen

- Ob indicates LOW level in the pad
- 1b indicates HIGH level in the pad

Wired interface registers have both configuration and session registers.

Session registers:

- ✓ Changes take effect immediately
- x Not persistent after reset

Configuration settings:

- ✓ Value remains valid after chip reset.
- X No immediate effect



9							Session	register addr	ess
		Block /	Address I <sup>2</sup> C	Byte 0 STATUS0_REG		Byte 1 Byte 2 Byte		Byte 3	
line		A0h	10A0h			STATUS1_REG	REG RFU		
	Bit		Name		Value	De	scription		
	-					VCC boot not done			
	/		VCC_BOOT_OK		1b	VCC boot done			
	6					NFC boot not done			
	0		NI 0_0001_01		1b	NFC boot done			
	5		ACTIVE NEC OK		0b	ALM RF not OK			
	5		ACTIVE_NEC_OR		1b	AKN RF OK			
	Δ	GPI	GPIO_PAD1_IN_STATUS			GPIO_1 input is LOW			
GFIU I	-					GPIO_1 input is HIGH			
	3	GPI	ο ραρό ινι στάτ	2115	0b	GPIO_0 input is LOW			
			GFIO_FADU_IN_STATUS		1b	GPIO_0 input is HIGH			
	2				0b	Only Passive Load Mo	odulation suppo	orted	
					1b	Active Load Modulation	on supported		
	1				0b	I2C interface not locked by arbiter			
					1b	Arbiter locked to I2C			
	0		NEC IE LOCKED		0b	NFC interface not locked by arbiter			
0					1b	Arbiter locked to NFC			

# LED example (output)

using FRDM-KW41Z and NTAG 5 Demo app



## Using GPIO features LED example

Description

- Using GPIO signal configured as output to switch ON / OFF LED present in FRDM-KW41Z board
- KW41Z shall be flashed so MCU dumps input signal to LED red channel\*
- Example available in NTAG 5 Demo app for mobiles
- OM2351OARD shall be connected to FRDM-KW41Z







\* No MCU would be needed in a final implementation

## Using GPIO features LED example

#### Step 1

19

• WRITE\_CONFIG command (C1h) over Configuration Bytes block (37h):







### Using GPIO features LED example

Step 2

• Change line state using PWM\_GPIO\_CONFIG\_REG



						Session	register ada
	Block Address			ss Byte 0		Byte 2	Byte 3
	A3h 10A3h		PWN CONF	/I_GPIO_ IG_0_REG	PWM_GPIO_ CONFIG_1_REG	RI	FU
Bit	it Name			Value	De	scription	
7	CDIO S			0b	Output status on pad i	s LOW	
/	GPIU_5	DA_PAD_001_51	ATU5	1b	Output status on pad i	is HIGH	
6				0b	Output status on pad i	s LOW	
0	GPIO_SCL_PAD_OUT_STAT		A103	1b	Output status on pad i	s HIGH	
5	GPIO	SDA PAD IN STA	SUTA	0b	Input status		
0	0110_		100	1b			
4	GPIO	SCL PAD IN STA	TUS	0b	Input status		
*	01101			1b	mparotatao		
3		GPIO SDA PAD		0b	Output		
				1b	Input		
2		GPIO_SCL_PAD		0b	Output		
-				1b	Input		
1	GPI	0_PWM1_SDA_P	٩D	0b	GPIO		
9.93		ere constant de la co	( <i>U</i> Prous	1b	PWM		
0	GPI	O_PWM0_SCL_P/	AD	0b	GPIO		
	0			1b	PWM		

### **Using GPIO features LED example: Signal generation**

1. Signal is generated by NTAG 5 depending on the register dedicated to control the GPIO 1. KW41Z monitors the signal generated by the NTAG 5 and dumps its value to turn ON/OFF LED 3.



### Using GPIO features LED example: Signal generation

1. Signal is generated by NTAG 5 depending on the register dedicated to control the GPIO 1. KW41Z monitors the signal generated by the NTAG 5 and dumps its value to turn ON/OFF LED 3

GND-

GPIO 0

GPIO 1

AG 5

2. User can control the level state of the signal and therefore the LED by writing to the specific register in NTAG 5 memory.





Evaluation board image is <u>NOT</u> the final one



# **Toggle button example (input)**

using FRDM-KW41Z and NTAG 5 Demo app



## Using GPIO features Toggle button example

#### Description

- Using GPIO signal configured as input to monitor button state
- Toggle button emulated using SW3 and SW4 buttons from FRDM-KW41Z
- KW41Z shall be flashed so MCU changes signal state depending on button clicked
- Example available in NTAG 5 Demo app for mobiles
- OM2351OARD shall be connected to FRDM-KW41Z





## Using GPIO features Toggle button example



				Session re	egister addres.	
Block A	ddress	Byte 0	Ryte 1	Byte 2	Byte 3	
IFC	I <sup>2</sup> C	5,000	byte i	5,102	Dyte o	
\0h	10A0h	STATUS0_REG	STATUS1_REG	RF	Ū	

Bit	Name	Value	Description
7	VCC POOT OK	0b	VCC boot not done
/	Vec_8001_0K	1b	VCC boot done
6	NEC POOT OK	0b	NFC boot not done
0	NFC_BOOT_OK	1b	NFC boot done
F		0b	ALM RF not OK
5	ACTIVE_NFC_OK	1b	ALM RF OK
4	GPIO_PAD1_IN_STATUS	0b	GPIO_1 input is LOW
4		1b	GPIO_1 input is HIGH
2	GPIO_PADO_IN_STATUS	0b	GPIO_0 input is LOW
5		1b	GPIO_0 input is HIGH
2		0b	Only Passive Load Modulation supported
2	ALIVI_PLIVI	1b	Active Load Modulation supported
1		0b	I2C Interface not locked by arbiter
	120_IF_EOCKED	1b	Arbiter locked to I2C
0		0b	NFC interface not locked by arbiter
U	NFU_IF_LUCKED	1b	Arbiter locked to NFC



1. Signal is generated by the KW41Z and rooted to the GPIO 1 pin of the NTAG 5 Eval board









Evaluation board image is <u>NOT</u> the final one

GPIO 1

- 1. Signal is generated by the KW41Z and rooted to the GPIO 1 pin of the NTAG 5 Eval board
- 2. If user clicks SW3 button, KW41Z turns the signal level to low state.



GPIO 1 (input) SW3 clicked





Evaluation board image is <u>NOT</u> the final one

GND-

GPIO 0

GPIO 1

- 1. Signal is generated by the KW41Z and rooted to the GPIO 1 pin of the NTAG 5 Eval board
- 2. If user clicks SW3 button, KW41Z turns the signal level to low state.
- 3. If user clicks SW4 button, the microcontroller will turn the signal level back to high







Evaluation board image is <u>NOT</u> the final one

- 1. Signal is generated by the KW41Z and rooted to the GPIO 1 pin of the NTAG 5 Eval board
- 2. If user clicks SW3 button, KW41Z turns the signal level to low state.
- 3. If user clicks SW4 button, the microcontroller will turn the signal level back to high
- 4. User can sense and monitor the state of GPIO input pad at any moment through NFC GPIO 1

#### GPIO 1 (input)





GND

GPIO 0



Evaluation board image is <u>NOT</u> the final one

# **Using PWM features**



### Using PWM features Configuring wired interface

Step 1

• WRITE\_CONFIG command (C1h) over Configuration Bytes block (37h):



#### public static final byte[] cmd\_activateGPIOPWM = new byte[]{





### Using PWM features Defining pads purposes and PWM parameters

#### Step 2

- Configure pads as PWM
- Configure pre-scale and resolution for PWM signals

	3		
Bit	Name	Value	Description
7		0b	Output status on pad is LOW
/	GFI0_SDA_FAD_001_STAT05	1b	Output status on pad is HIGH
6		0b	Output status on pad is LOW
0	GPI0_SUL_PAD_001_STATUS	1b	Output status on pad is HIGH
E		0b	Inputatotua
5	5 GFIO_SDA_FAD_IN_STATOS		Inputstatus
1	GPIO_SCL_PAD_IN_STATUS	0b	Inputatotua
4		1b	Inputstatus
2		0b	Output
5	GFIO_SDA_FAD	1b	Input
2		0b	Output
2	GFIO_SCL_FAD	1b	Input
1		0b	GPIO
1	GFIU_FWWWIT_SDA_PAD	1b	PWM
0		Ob	GPIO
0	GFIO_FWWW0_SCL_PAD	1b	PWM

						Session	register add		
E	Block Address		Block Address		Byte (		Byte 1	Byte 2	Byte 3
NF							_,		
39	h	1039h	PWM_GF	PIO_	PWM_GPIO_		=1.1		
A3	ßh	10A3h	CONFIG_0	_REG	CONFIG_1_REG	κ.	-0		
		· ·							
	Bit Name			Value	De	scription			
	6-7	PWM1_PRESCALE		00b	Pre-scalar configuration for PWM1 channel (default 00h)				
	4-5	PWM0_PRE	SCALE	00b	Pre-scalar configuration for PWM0 channel (default 00h)				
				00b	6-bit resolution (defa	ault)			
L	2-3			01b	8-bit resolution				
L	2-5	F WWIT_RESOLU		10b	10-bit resolution				
				11b	12-bit resolution				
					6-bit resolution				
	0-1	PWM0 RESOLUT	TION CONF	01b	8-bit resolution	8-bit resolution			
				10b	10-bit resolution				
				11b	12-bit resolution				

For more information about PWM signal parameters and generation, please refer to application note AN11203



### Using PWM features Changing start time and duty cycle

#### Step 3

• Configure time for rising and falling edge. This can be calculated out of the start time and duty cycle parameters:

PWMx\_ON:

Start time = 2<sup>Resolution</sup>x Start time<sub>%</sub>

PWMx\_OFF:

End time =  $2^{\text{Resolution}}x$  (Start time<sub>%</sub> + Duty cycle)

Equivalent register for Channel 1 is found in addresses:

- 3Bh (configuration settings)
- A5h (session register)

					Sessio	n register address					
B	lock Address		Byte 0	Byte 1	Byte 2	Byte 3					
NF	C I <sup>2</sup> C	:	byteo	byter	byte 2	Dyte 5					
ЗA	h 103,	۹h									
A4	h 10A	4h	PVVIVIU_	UN_REG	PVVIVIU_C	JFF_REG					
			F			_					
Bit	Name	Value		Description							
12-15	RFU	All Ob									
0-11	PWM0_ON	All Ob	Coded time PW	'M channel 0 output	will be asserted HIG	βH					
Bit	Name	Value		Description							
12-15	RFU	All Ob									
0-11	PWM0_OFF	All Ob	Coded time PW	M channel 0 output	will be asserted LOV	N					





# LED intensity example

using FRDM-KW41Z and NTAG 5 Demo app



## Using PWM features LED intensity example

#### Description

- Uses PWM signal to control intensity of two LEDs present in FRDM-KW41Z board using signal duty cycle
- Signal is generated using four different parameters
- Example available in NTAG 5 Demo app for mobiles
- KW41Z shall be flashed so microcontroller roots signal to LEDs input.
- OM2351OARD shall be connected to FRDM-KW41Z





### Using PWM features LED intensity example

- 1. User changes PWM signal parameters
- 2. When user clicks on 'Write config' application gathers all information and sends commands to re-configure PWM signal:

Flags	WRITE_CONF	Manuf. Code	UID (optional)	Block Address	Data	CRC16
12h	C1h	04h		A3h		Auto

Flags	WRITE_CONF	Manuf. Code	UID (optional)	Block Address	Data	CRC16
12h	C1h	04h		A4h		Auto

Flags	WRITE_CONF	Manuf. Code	UID (optional)	Block Address	Data	CRC16
12h	C1h	04h		A5h		Auto

Configure pads as PWM Define pre-scale and resolution

Configure rising/falling edge for Channel 0 (LED 3)

Configure rising/falling edge for Channel 1 (LED 4)



### Using PWM features LED intensity example: Signal generation

 Signal is generated by NTAG 5 depending on the register dedicated to control each PWM channel. KW41Z monitors the signal generated by the NTAG 5 and dumps its value to the input of the respective LED.



PWM 0

37 Training Knowledge

LED3



### **Using PWM features** LED intensity example: Signal generation

GND ----

PWM 0

PWM 1

AG 5

**dXN** 

- 1. Signal is generated by NTAG 5 depending on the register dedicated to control each PWM channel. KW41Z monitors the signal generated by the NTAG 5 and dumps it value to the input of the respective LED.
- 2. User can change the intensity of the LED by writing to the related session register and modify the duty cycle of the generated PWM signal



#### PWM 0



# Using pass-through mode



### Using pass-through mode Introduction

- Pass through mode transfers data from RF to I2C interface and vice versa using the 256-byte SRAM saving EEPROM cycles. Available for NTAG 5 link and boost models.
- Data flow from one side to the other is synchronized using interruption signal and register settings.

#### Use cases:

- RF  $\rightarrow$  I2C data exchange:
- Mobile device writes data into the microcontroller
- Update microcontroller FW from NFC interface
- I2C  $\rightarrow$  RF data exchange:
- Download of data into mobile device (e.g., large amount of logging data, error descriptions...)







### Using pass-through mode Configuration (I)

41

WRITE\_CONFIG command (C1h) over Configuration Bytes block (37h):

**@Override** public void onClick(DialogInterface dialog, int which) { byte[] response = sendCommand(cmd activateI2CSlave); if (response != null) showConfirmationSnackbar();

#### public static final byte[] cmd activateI2CSlave = new byte[]{





## Using pass-through mode Configuration (II)

#### Requirements

- 1. NFC\_FIELD\_OK = 1b  $\rightarrow$  bit0 of STATUS0\_REG
- 2. VCC\_SUPPLY\_OK = 1b  $\rightarrow$  bit1 of STATUSO\_REG
- 3. SRAM\_ENABLE = 1b  $\rightarrow$  bit1 of CONFIG\_1

#### Data flow direction

- PT\_TRANSFER\_DIR → bit2 of STATUSO\_REG
- ED pin to notify when last SRAM page was read/written

Accessing SRAM

- <u>RF perspective</u>
   SRAM\_READ and SRAM\_WRITE over addresses 00h-3Fh
- <u>I2C perspective</u>

READ / WRITE over addresses 2000h-203Fh



Block Address		Byte 0	Byte 1	Byte 2	Byte 3
NFC	I <sup>2</sup> C	byte o	byter	byte 2	Dyte o
A0h	10A0h	STATUS0_REG	STATUS1_REG	RI	FU

Block Address		Byte 0	Byte 1	Byte 2	Byte 3
37h	37h 1037h CONFIG_0		CONFIG_1	CONFIG_2	RFU





# **Pass-through example**

using FRDM-KW41Z and NTAG 5 Demo app



#### Description

- Uses pass-through feature to exchange pre-defined data with KW41Z
- Wired interface must be configured in I<sup>2</sup>C slave mode to communicate with KW41Z using I<sup>2</sup>C interface.
- Example available in NTAG 5 Demo app for mobiles
- KW41Z shall be flashed so microcontroller roots signal to LEDs input.
- OM2351OARD shall be connected to FRDM-KW41Z





#### NO Continue LOOP? while(continueLoop) { Exit Loop Read byte[] responseTagStatus = sendCommand(cmd readTagStatus); TagStatus (A0) PT\_TRSF\_DIR YES NO if (Parser.IsBitSet(responseTagStatus[1], 2)) { $RF \rightarrow I^2C?$ NO NO All write iterations? All read iterations? if (writeCounter < SRAM LOOP SIZE) {</pre> NO NO SRAM\_DATA\_READY? SRAM\_DATA\_READY if (!Parser.IsBitSet(responseTagStatus[1], 5)) { WriteSRAM ReadSRAM responseWriteSRAM = sendCommand(finalCommandWriteSRAM);

Block diagram

## Using pass-through mode Pass-through example

 $\mathsf{RF} \twoheadrightarrow \mathsf{I}^2\mathsf{C}$ 

 NFC device writes in NTAG 5 SRAM memory. KW41Z detects that PT\_TRANSFER\_DIR indicates RF→I2C direction, turns LED in blue and waits until SRAM is available to be read.





 $\mathsf{RF} \twoheadrightarrow \mathsf{I}^2\mathsf{C}$ 

- NFC device writes in NTAG 5 SRAM memory. KW41Z detects that PT\_TRANSFER\_DIR indicates RF→I2C direction, turns LED in blue and waits until SRAM is available to be read.
- When NFC device finishes writing KW41Z starts reading from SRAM. LED remains in blue until PT\_TRANSFER\_DIR changes to I<sup>2</sup>C→RF.





 $I^2C \rightarrow RF$ 

 KW41Z starts writing in NTAG 5 SRAM memory and turns LED in green. NFC device detects that PT\_TRANSFER\_DIR indicates I2C→RF direction and waits until SRAM is available to be read.





 $I^2C \rightarrow RF$ 

- KW41Z starts writing in NTAG 5 SRAM memory and turns LED in green. NFC device detects that PT\_TRANSFER\_DIR indicates I2C→RF direction and waits until SRAM is available to be read.
- When KW41Z finishes writing NFC device starts reading from SRAM. LED remains in green until PT\_TRANSFER\_DIR changes to I<sup>2</sup>C→RF.





LED

# Using I<sup>2</sup>C Master mode



### Using I<sup>2</sup>C Master mode Introduction

- I2C Master mode allows users to execute I2C commands directly from an NFC device by creating a transparent I2C channel with devices working as I2C slave.
- Working in I2C master mode, different I2C slave devices (e.g., sensors) can be connected without a microcontroller.
- Needed power for the sensors can be provided with NTAG 5 energy harvesting capabilities.





## Using I<sup>2</sup>C Master mode Configuration

WRITE\_CONFIG command (C1h) over Configuration Bytes block (37h):







Detailed information on how to configure I2C master channel and I<sup>2</sup>C clock speed can be found in AN12368  $\,$ 



### Using I<sup>2</sup>C Master mode Sending Read/Write I2C commands

#### Writing to I<sup>2</sup>C interface

• Write\_I2C command (D4h)  $\rightarrow$  Writes command into I2C line. Includes I2C address of the target slave

Flags	WRITE I <sup>2</sup> C	Manuf. Code	UID (optional)	I <sup>2</sup> C Param	Data length N	Data	CRC16
8 bits	D4	8 bits	64 bits	8 bits	8 bits	(N+1) x 8 bits	16 bits

#### Reading from I<sup>2</sup>C interface

• Read\_I2C command (D5h)  $\rightarrow$  Reads data from I2C line and transfer it into NTAG 5 SRAM

Flags	READ I <sup>2</sup> C	Manuf. Code	UID (optional)	I <sup>2</sup> C Param	Data Length N	CRC16
8 bits	D5	8 bits	64 bits	8 bits	8 bits	16 bits

#### Reading from SRAM memory

• Read SRAM command (D2h) → Reads data from NTAG 5 SRAM memory

Flags	Read SRAM	Manuf. Code	UID (optional)	Block Address	Number of blocks	CRC16
8 bits	D2	8 bits	64 bits	8 bits	8 bits	16 bits





## I<sup>2</sup>C Master mode example

using FRDM-KW41Z and NTAG 5 Demo app



### Using I<sup>2</sup>C Master mode I<sup>2</sup>C Master mode example

#### Description

- Allows user to directly send I2C commands to FXOS8700CQ accelerometer and magnetometer sensor present in FRDM-KW41Z board.
- User can send a default command from a list or introduce a customized command









### Using I<sup>2</sup>C Master mode I<sup>2</sup>C Master mode example







Э*1* 

### Using I<sup>2</sup>C Master mode I<sup>2</sup>C Master mode example

Example: Get temperature from sensor

• Step 3: Reading content from NTAG 5 SRAM:









# More support



#### More support Relevant resources regarding NTAG 5 family

#### NTAG 5 switch website

https://www.nxp.com/products/rfid-nfc/nfc-hf/ntag/nfc-tags-for-electronics/ntag-5-switch-nfc-forumcompliant-pwm-gpio-bridge-for-lighting-and-gaming:NTAG5-SWITCH

#### > NTAG 5 link website

https://www.nxp.com/products/rfid-nfc/nfc-hf/ntag/nfc-tags-for-electronics/ntag-5-link-nfc-forumcompliant-ic-bridge-for-iot-on-demand:NTAG5-LINK

#### NTAG 5 boost website

https://www.nxp.com/products/rfid-nfc/nfc-hf/ntag/nfc-tags-for-electronics/ntag-5-boost-nfc-forumcompliant-ic-bridge-for-tiny-devices:NTAG5-BOOST

#### NTAG 5 development kit

http://www.nxp.com/products/rfid-nfc/nfc-hf/ntag/ntag-5-development-kit:OM23510ARD

#### > NXP Tech community

https://www.nxp.com/support/support:SUPPORTHOME







#### MobileKnowledge

MobileKnowledge is a team of HW, SW and system engineers, experts in **smart, connected and secure** technologies for the IoT world. We are your ideal **engineering consultant** for any specific support in connection with your **IoT** and **NFC** developments. We design and develop secure HW systems, embedded FW, mobile phone and secure cloud applications.

Our services include:

- Secure hardware design
- Embedded software development
- NFC antenna design and evaluation
- NFC Wearable
- EMV L1 pre-certification support
- Mobile and cloud application development
- Secure e2e system design

www.themobileknowledge.com mk@themobileknowledge.com





We help companies leverage the secure IoT revolution





#### NTAG 5 Webinar series – Product Support Package

Pablo Fuentes (Speaker) Angela Gemio (Host)

> Time for Q & A





#### NTAG 5 Webinar series – Product Support Package

#### Thank you for your kind attention!

Please remember to fill out our evaluation survey (pop-up)

Check your email for material download and on-demand video addresses

## Please check NXP and MobileKnowledge websites for upcoming webinars and training sessions

http://www.nxp.com/support/classroom-training-events:CLASSROOM-TRAINING-EVENTS www.themobileknowledge.com/content/knowledge-catalog-0





#### MobileKnowledge

MobileKnowledge is a team of HW, SW and system engineers, experts in **smart, connected and secure** technologies for the IoT world. We are your ideal **engineering consultant** for any specific support in connection with your **IoT** and **NFC** developments. We design and develop secure HW systems, embedded FW, mobile phone and secure cloud applications.

Our services include:

- Secure hardware design
- Embedded software development
- NFC antenna design and evaluation
- NFC Wearable
- EMV L1 pre-certification support
- Mobile and cloud application development
- Secure e2e system design

www.themobileknowledge.com mk@themobileknowledge.com





We help companies leverage the secure IoT revolution

