



**PN7462 family - first all-in-one full NFC solution**  
**NFC + MCU + CT + SW in one chip**

MobileKnowledge  
April 2016

# Agenda

## Session 13<sup>th</sup> April: **PN7462 family introduction**

- ▶ Positioning within the NFC portfolio and overview
- ▶ Target markets and benefits
- ▶ PN7462 family derivatives
- ▶ Detailed product description and key features
- ▶ OM27460CDK development kit and product support package
- ▶ Ordering details

## Session 20<sup>th</sup> April: **PN7462 product support package**

- ▶ Product support package details
- ▶ OM27462CDK development kit
- ▶ PN7462AU hardware overview
- ▶ PN7462 SW architecture and SW development environment
- ▶ PN7462 NFC Cockpit

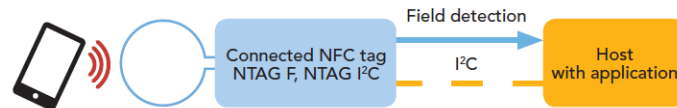
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# PN7462 family within the NFC product portfolio

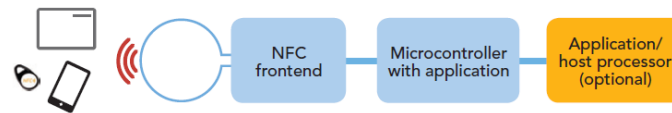
## Connected NFC tag solutions

Our connected NFC tag solutions include a NFC Forum RF interface, an EEPROM, and a field-detection function (NTAG F) or a field-detection function with an I<sup>2</sup>C interface. **NTAG F, NTAG I<sup>2</sup>C, NTAG I<sup>2</sup>C plus**



## NFC frontend solutions

Our standalone frontends, which work seamlessly with the NFC Reader Library, are the most flexible way to add NFC to a system. **PN512, CLRC633, PN5180**

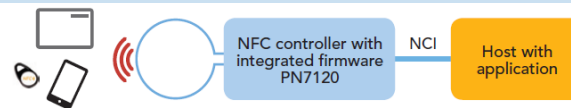


## NFC controller solutions

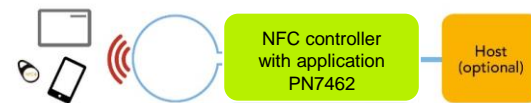
Our NFC controller solutions enable higher integration with fewer components combining an NFC frontend with an advanced 32-bit microcontroller. **PN533, PN7120**

Options include integrated firmware, for an easy, standardized interface, or a **freely programmable microcontroller with the ability to load fully-custom applications**. **PR601, PN7462**

### Integrated firmware



### Customizable firmware



# PN7462 family combines NXP expertise into a one-chip solution

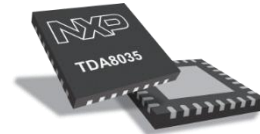
Low power Cortex M0 core controller with USB



**Single chip solution** for contact, contactless & NFC with a large flash user memory saving cost and space



NXP creator of the market reference with TDA80xx family. More than 1B devices sold



NXP world leader with NFC contactless technology



# PN7462 family - first all-in-one full NFC solution



## PN7462 family

- State of the art RF interface, compliant with: ISO/IEC 14443, ISO/IEC 18092, ISO/IEC 15693, ISO/IEC 18000-3M3, FeliCa
- Contact interface compliant with ISO/IEC 7816-2 to 4
- Integrated 20MHz Cortex M0 microcontroller with 80/160kB flash memory, 12kB RAM and 4kB EEPROM
- One configurable host interface: I<sup>2</sup>C, SPI, USB, HSUART
- Two master interfaces: I<sup>2</sup>C and SPI
- 12 to 21 GPIOs
- DPC for optimized antenna performance
- EMVCo and NFC Forum compliance for easy certification
- Advanced power management
- Extensive support tools, including sample source code
- HVQFN64 package (9x9 mm)

**NFC and contact  
interfaces, MCU,  
and software  
in one chip**

# PN7462 family key benefits



## Outstanding RF performance

- Dynamic power control (DPC) maximizes performance in detuned conditions
- Transmitter current up to 250mA
- Active and passive load modulation support



## Ease of integration

- Power supply from 2.7 to 5.5V
- Multiple host interfaces
- GPIOs and master drivers for peripherals
- Protected firmware download in flash



## Flexibility in development

- Easy configuration
- Multiple SW examples provided for each use case
- EMVCo compliant libraries
- NFC Forum compliant libraries
- Usage of standard development tools



## Optional contact reader

- Class A,B and C cards supported
- Fully integrated ISO/IEC 7816-3&4 UART
- Baud rate up to 1 Mbps
- Capability to drive external frontends for SAMs

# PN7462 target markets

## Physical access control

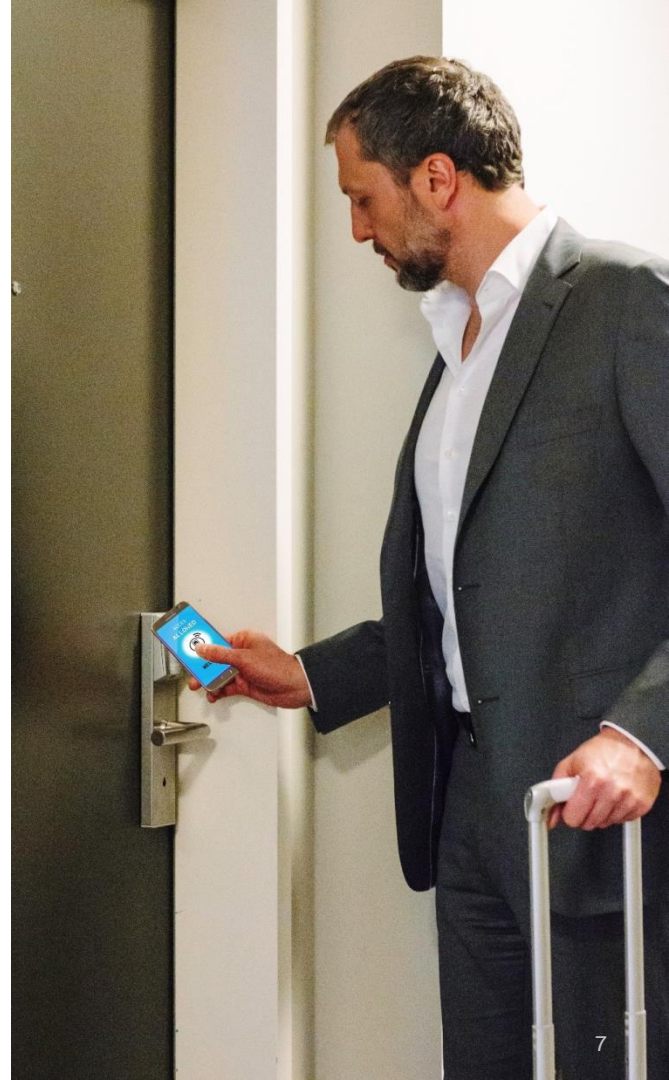
- **Single chip solution** for stand alone readers
- **Low power management** to enable battery operated operation
- **Full NFC** enabling communication with cards and phones

## Home banking

- **Single chip solution** – USB, contact and contactless interfaces
- **EMVCo L1 compliance** for interoperability with payment cards

## Multimarket USB readers

- **Highly customizable** interfaces
- **Complete support package** with NFC Forum and EMVCo compliant SW library
- **Source code** of typical applications



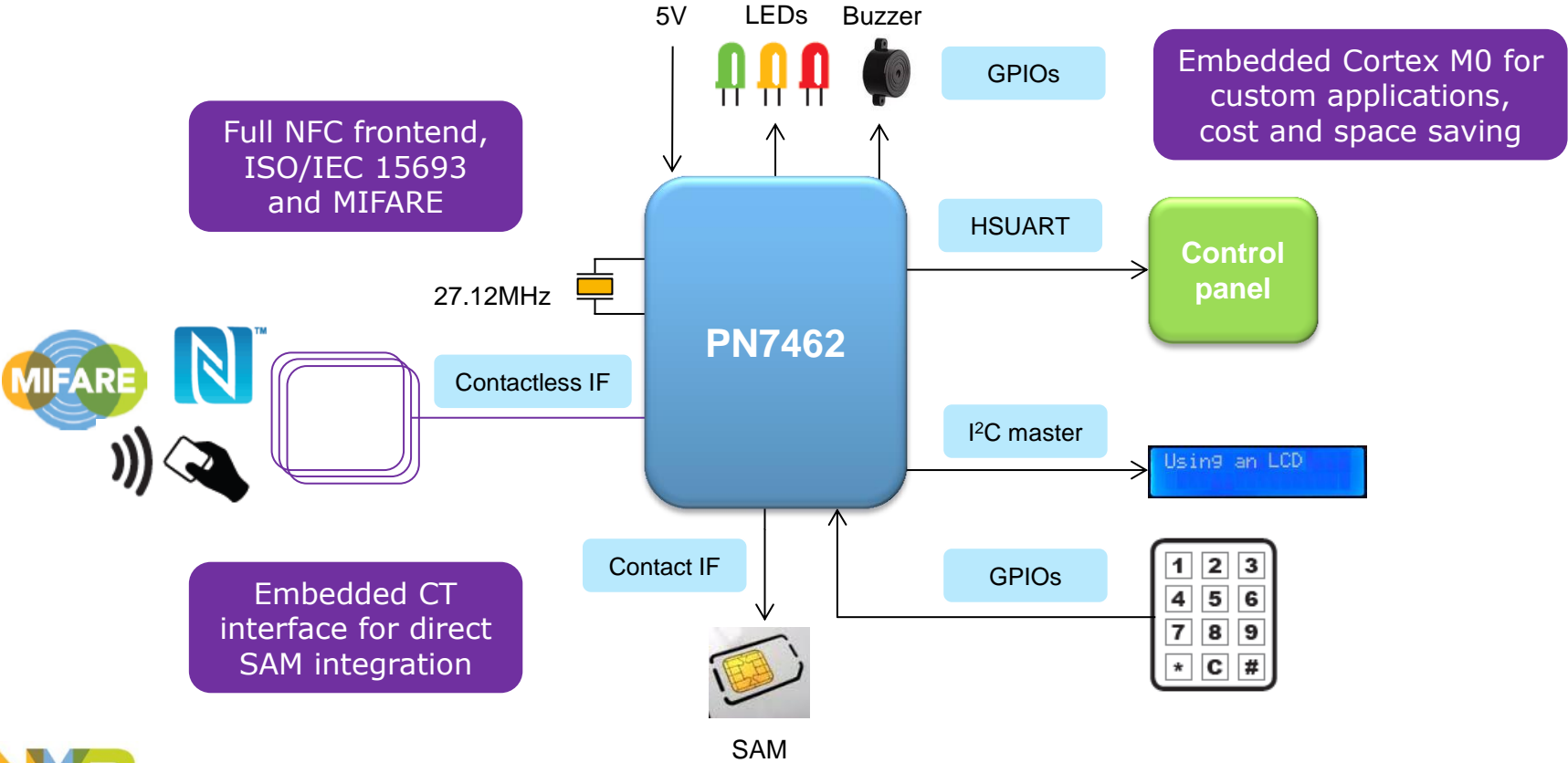
# PN7462 family is the solution for your application

Typical applications	PN7462	PN7362	PN7360	
Corporate access	✓	✓	✓	
Hospitality (access)		✓	✓	
Payment terminal	✓			
Home banking	✓			
USB reader		✓	✓	
Gaming console accessories		✓	✓	
NFC enabled board game		✓	✓	
	160 kB	160 kB	80 kB	Flash
	✓			Contact reader
	PN7462	PN7362	PN7360	<b>Features</b>

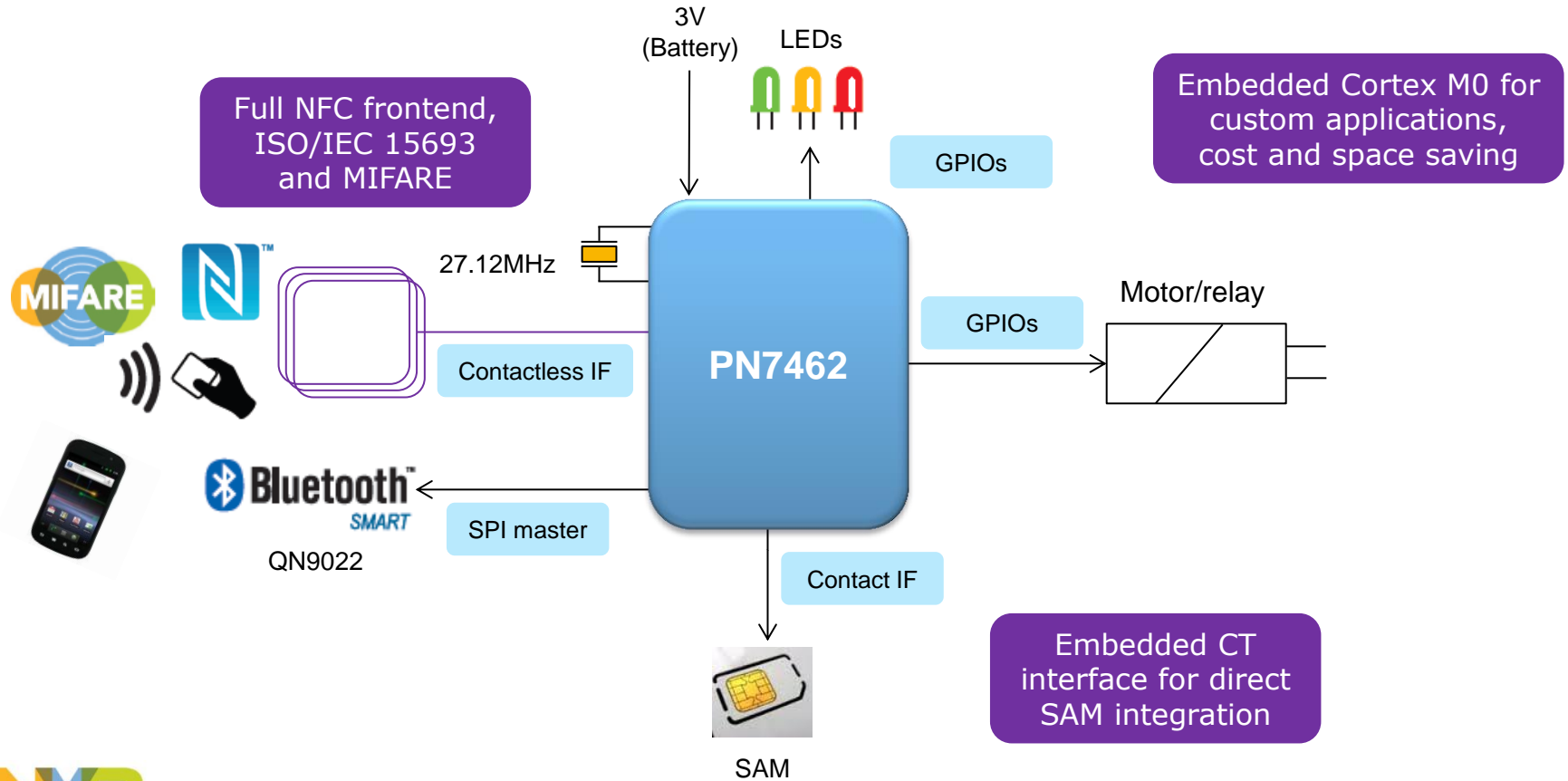




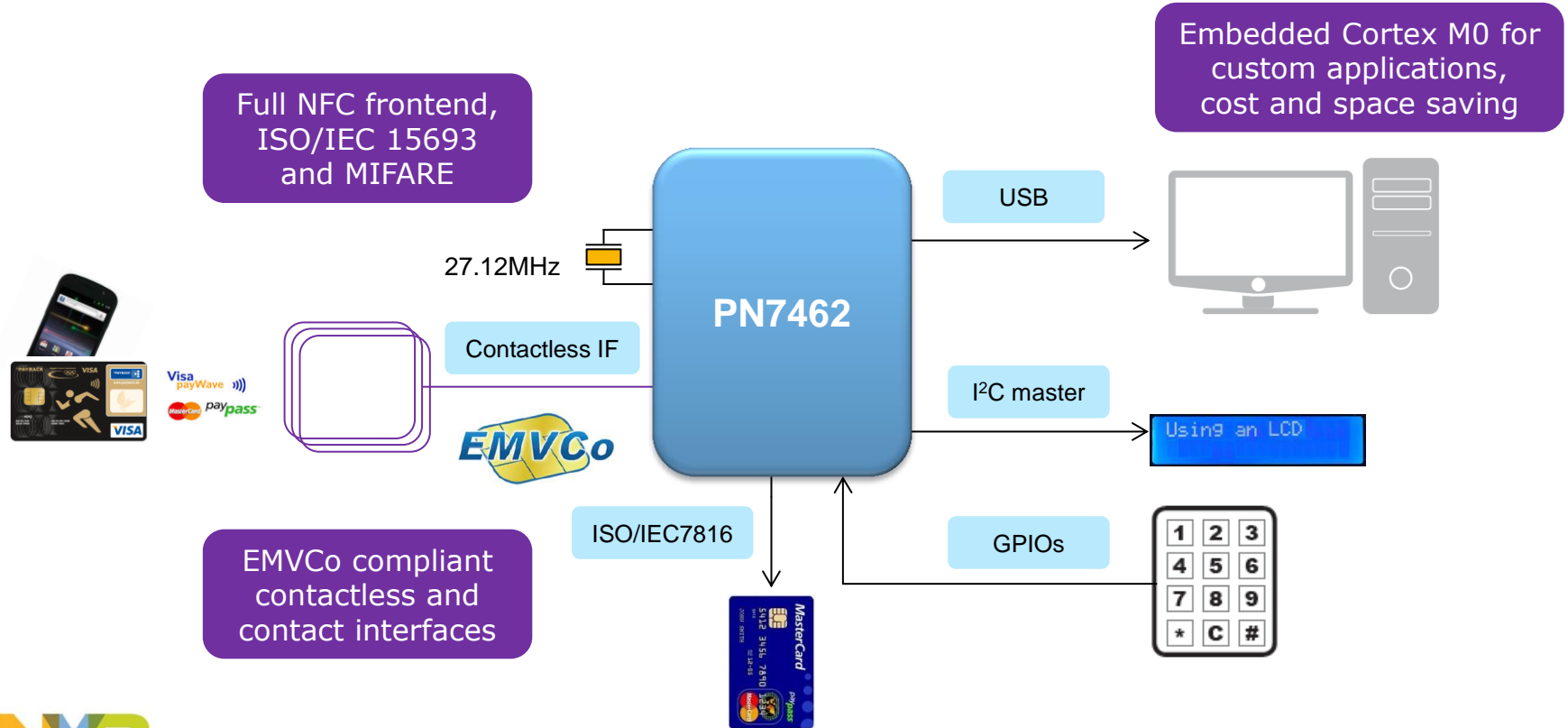
# PN7462 for corporate access



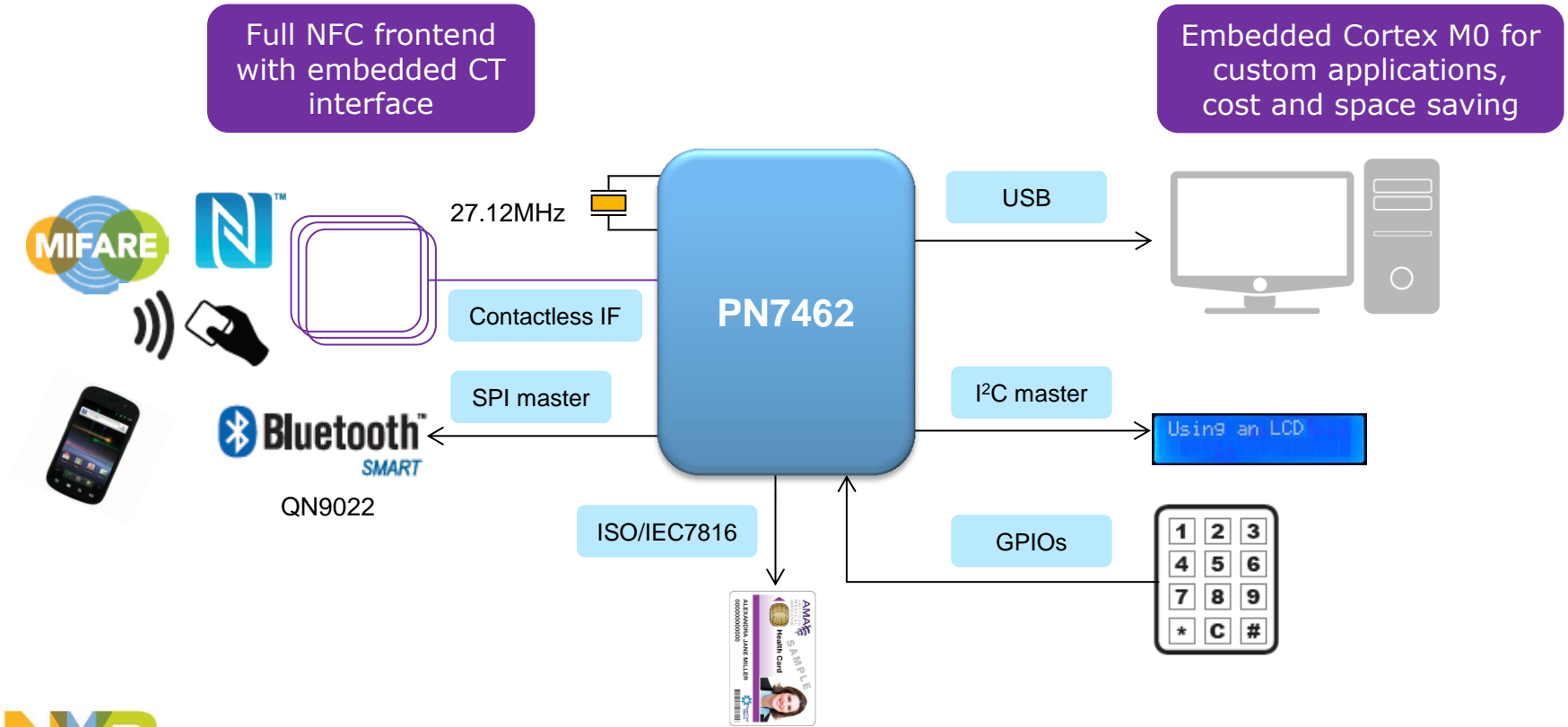
# PN7462 for hospitality



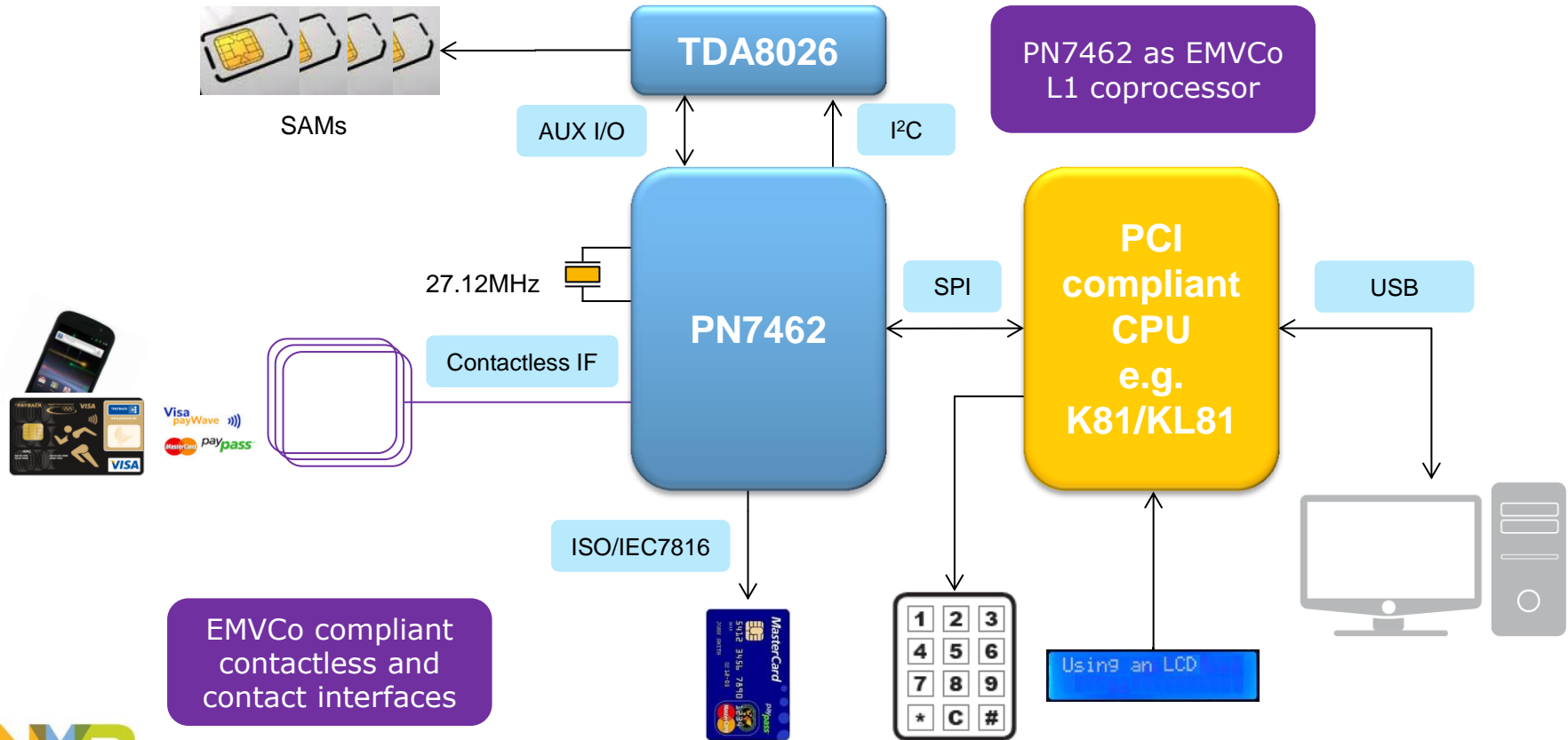
# PN7462 for home banking



# PN7462 for USB reader



# PN7462 as a payment coprocessor for POS system



# Positioning PN7462 family

# Positioning PN7462 family

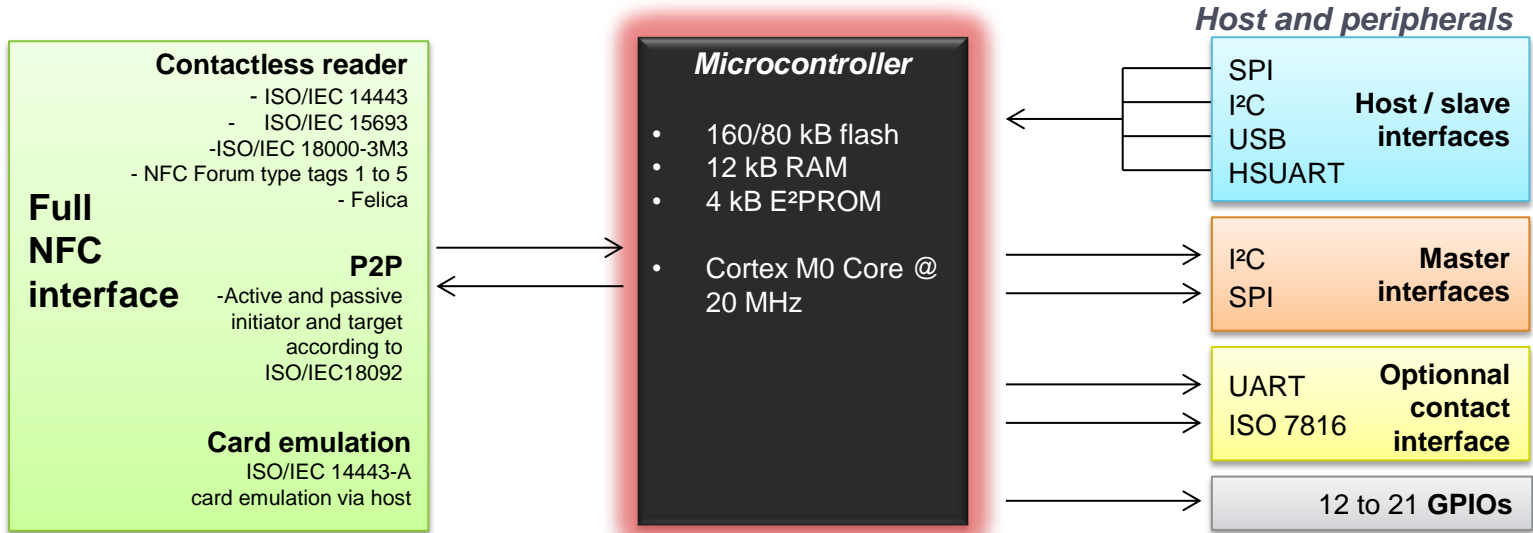
	Card mode in host	Reader & Writer mode		Peer-to-Peer mode	NFC Forum compliance	EMVCo PCD protocol	Embedded MCU	Dynamic Power Control	ISO/IEC 7816 interface
<b>PR601</b>		MIFARE, ISO/IEC 14443-A&B, FeliCa	ISO/IEC15693 ISO/IEC 18000-3M3	Passive initiator		Yes	Yes customizable FW		
<b>PN7120</b>	ISO/IEC 14443 A&B	MIFARE, ISO/IEC 14443-A&B, FeliCa	ISO/IEC15693 ISO/IEC 18000-3M3	Active & Passive	Yes	Yes	Yes no rewritable FW		
<b>PN5180</b>	ISO/IEC 14443A	MIFARE, ISO/IEC 14443-A&B, FeliCa	ISO/IEC15693 ISO/IEC 18000-3M3	Active & Passive	Yes	Yes		Yes	
<b>PN7462</b>	ISO/IEC 14443A	MIFARE, ISO/IEC 14443-A&B, FeliCa	ISO/IEC15693 ISO/IEC 18000-3M3	Active & Passive	Yes	Yes	Yes, customizable FW	Yes	Class A, B C

**PN7462**

**Product description**



# PN7462 feature overview



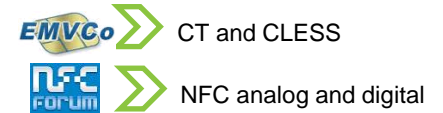
## Additional features

- ▶ **Integrated voltage monitoring** for battery operated devices
- ▶ **Low Power Card Detection**
- ▶ **SWD or integrated USB mass storage** (primary downloader) for code download

## Package HVQFN64



## Standard compliance



# PN7462 technical product features

## Features

### CPU core

- ▶ Cortex M0 160kB flash, 12kB RAM, CPU-clk = 20MHz

### RF performance

- ▶ Transmitter current up to 250mA
- ▶ Dynamic Power Control

### Ease of integration

- ▶ Multiple host interfaces
- ▶ GPIOs and master drivers for peripherals
- ▶ Protected firmware download in flash
- ▶ Temperature range: -40°C / +85°C

### Flexibility in development

- ▶ Ease of configuration
- ▶ Multiple SW examples provided for different use cases
- ▶ EMVCo validated libraries
- ▶ NFC Forum compliant libraries
- ▶ Usage of standard development tools

## Package

- ▶ HVQFN64

## RF communication modes

### Reader/Writer modes

- ▶ NFC Forum tag type 1 to 5
- ▶ ISO/IEC 14443 Type A & B R/W up to 848 kbit/s
- ▶ ISO/IEC 15693 reader (I-Code SLI)
- ▶ ISO/IEC 18000-3M3 reader (I-Code ILT)
- ▶ FeliCa tags up to 424kbps
- ▶ MIFARE 1K/4K
- ▶ MIFARE DESFire

### Card modes

- ▶ ISO/IEC 14443-4 card emulation

### P2P modes

- ▶ Active and passive initiator and target according ISO/IEC 18092 at all data rates

## Contact reader

- ▶ Class A, B, C card supported
- ▶ Fully integrated ISO/IEC 7816-3&4 UART
- ▶ Baud rate up to 1Mbit/s
- ▶ Capability to drive external frontend for SAMs

## Interfaces

- ▶ I<sup>2</sup>C/SPI/USB/UART host interfaces
- ▶ SPI and I<sup>2</sup>C master interfaces

# **Integrated contactless interface**

# PN7462 is compliant with all RF standards

## *High RF output power frontend IC for transfer speed up to 848 kbits/s*

- ▶ Output power: up to 250 mA
- ▶ DPC – Dynamic Power Control
- ▶ LPCD - Low Power Card Detection function
- ▶ Sensitivity increased by 2 compared to PN512. RF field-detection for wake-up in stand-by mode

## *Full NFC support*

- ▶ Full NFC Tag support (Type 1 to 5), P2P active and passive, target and initiator, card emulation ISO/IEC14443 type 4A
- ▶ Support ALM (active load modulation) and PLM (passive load modulation)

## *State of the art RF frontend - compliant with all RF standards*

- ▶ NFC Forum, ISO/IEC 14443 type A and type B, MIFARE family, ISO/IEC 15693 and ISO/IEC 18000-3 mode 3

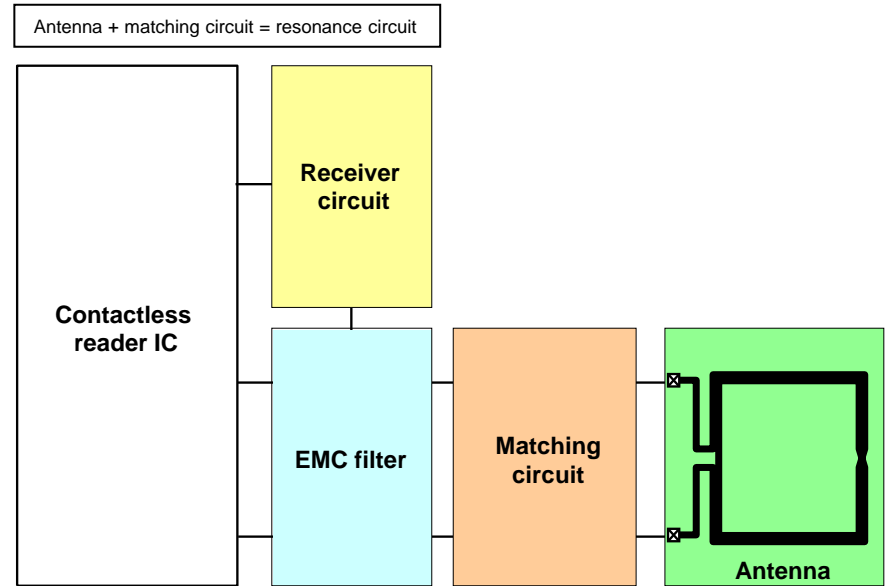
## *EMVCo compliant*

- ▶ Integrated EMD handling



# PN7462 NFC antenna tuning procedure

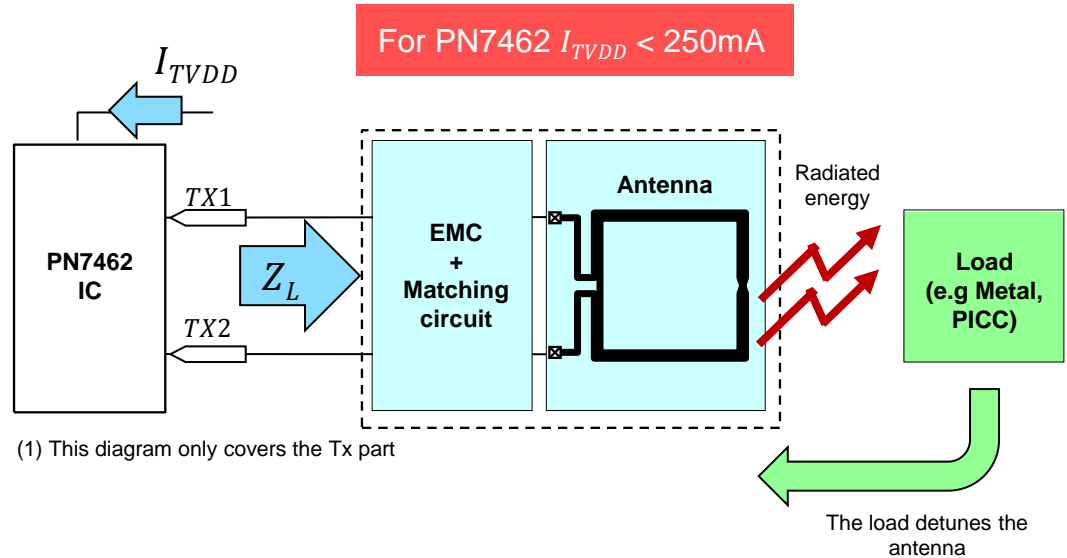
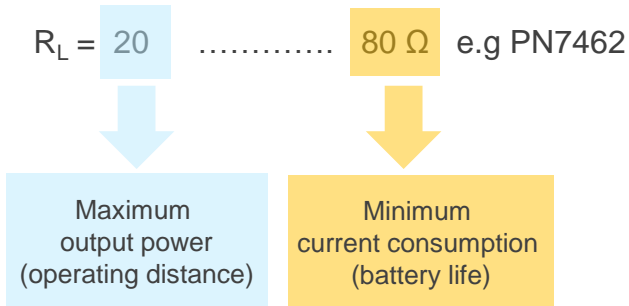
- 1** Measure antenna coil  
*Determine LCR values of the antenna coil*
- 2** Define target impedance and Q-factor  
*To optimize RF output power or battery life*
- 3** Define the EMC filter  
*Filtering of unwanted harmonics*
- 4** Calculate matching components  
*Using provided excel sheet*
- 5** Simulate the matching  
*Using matching simulation tools*
- 6** Assembly and measurement  
*Field measurement and fine tuning*
- 7** Adjust receiver circuit  
*Tuning reader sensitivity*



# PN7462 NFC antenna tuning procedure

## Define target impedance so that $I_{TVDD}$ does not exceed the IC limits (Step 2)

- ▶ We need to adjust the target impedance the NFC controller IC “sees” according to the performance we want to achieve.
  - Maximum output power
  - Minimum current consumption (battery life)
- ▶ The target impedance ( $R_L$ ) is chosen so that the highest possible output power does not exceed the maximum driver current ( $I_{TVDD}$ ).



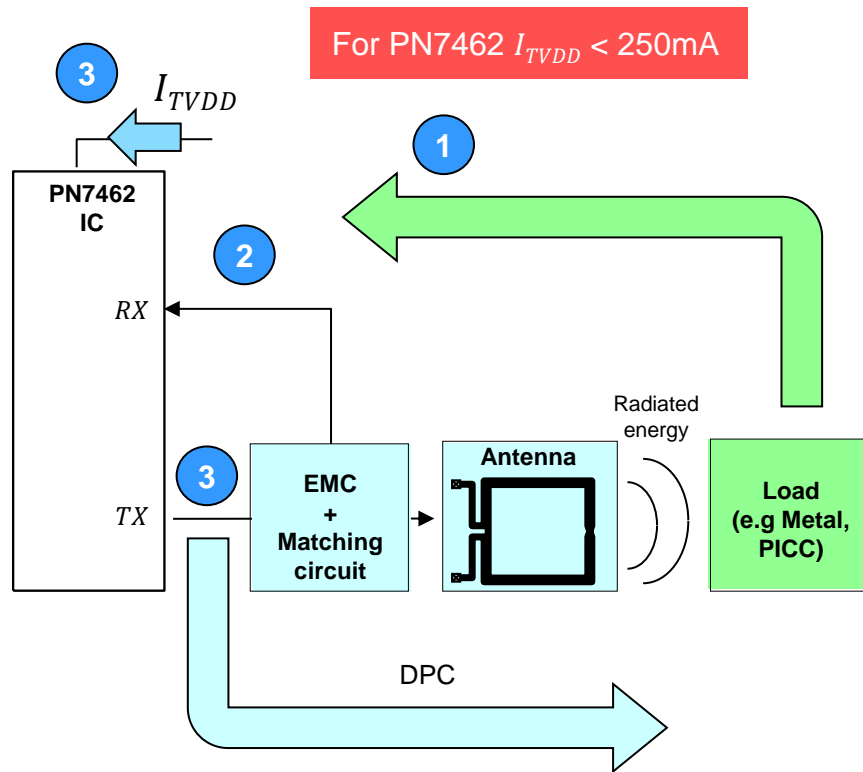
Different load detuning effect depending on “symmetric” or “asymmetric” antenna tuning

# Why do we need Dynamic Power Control (DPC)?

## “Symmetrical” antenna with DPC

- 1** A load change decreases the impedance, i.e. increases  $I_{TVDD}$
- 2** The DPC uses the changed Automated Gain Control (AGC) value to change TVDD settings
- 3** The changed TVDD settings reduce the  $I_{TVDD}$  and power and field strength

DPC uses gears to control the Tx output power and consequently, controls current / field strength



# Dynamic Power Control (DPC) at a glance

## Robust / Performance with DPC

Controls antenna current, RF power, and the related waveforms to deliver optimized RF performance, even under detuned conditions.

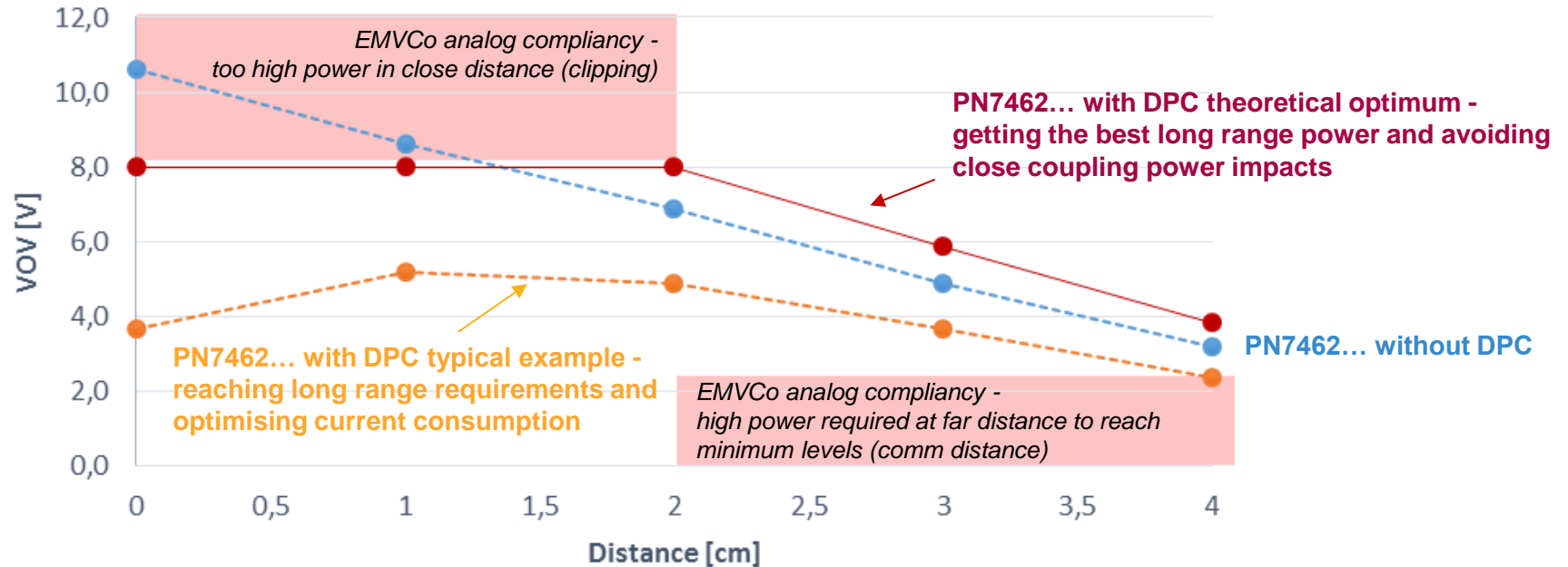
Maximizes the transmitter current during detuned conditions compensating for any negative effects generated by nearby metal, cards, or phones.

Controls the field strength along with the operating range, to stay within the ISO/IEC and EMVCo requirements

Ensures robust communication with smartcards and smartphones, without using any additional external components.



# Dynamic Power Control (DPC) in detail



# Integrated contact interface

# PN7462 - ISO/IEC 7816 UART & contact reader interface

## *Class A, B and C cards support (1.8 V, 3 V, 5 V)*

- ▶ Specific ISO UART, variable baud rate through frequency or division ratio
- ▶ Programming, error management at character level for T=0, extra guard time register
- ▶ DC/DC converter for Class A support starting at 3 V, and Class B support starting 2.7V
- ▶ Clock generation up to 13.56 MHz
- ▶ Synchronous card support



## *Card and reader protections*

- ▶ Thermal and short-circuit protection on all contact cards
- ▶ Automatic activation and deactivation sequence: initiated by software or by hardware in case of short-circuit, card take-off, overheating, VDD or VDD drop-out
- ▶ Enhanced ESD protection (>8 kV)



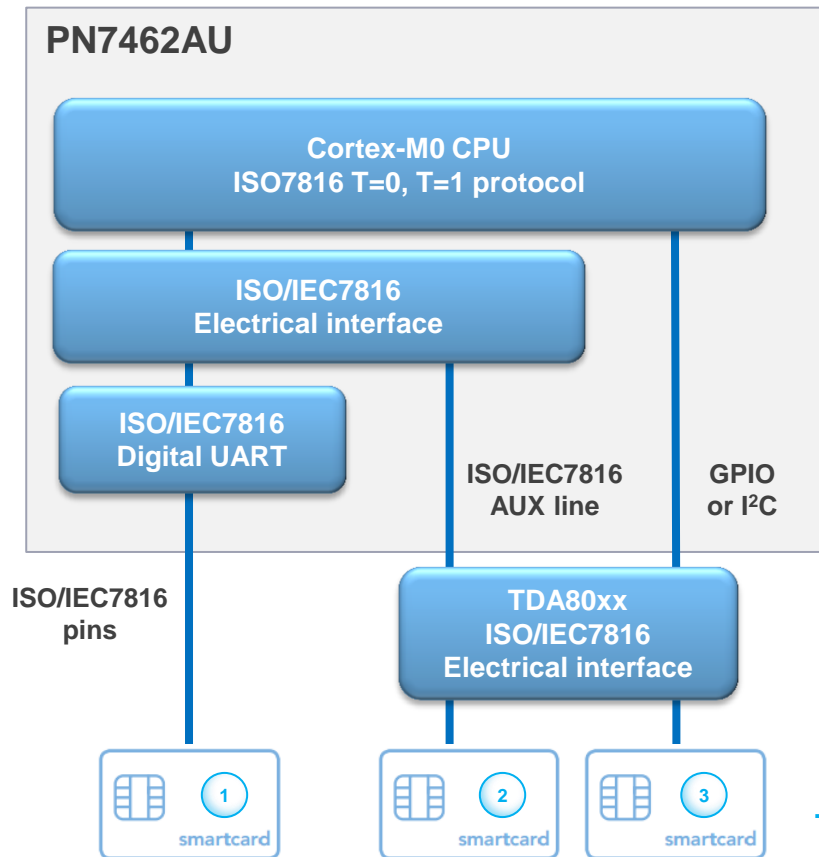
## *ISO/IEC 7816 compliance and EMVCo 4.3 compliance*

### *IO/AUX interface*

- ▶ Possibility to extend the number of contact interface adding a slot extender like TDA8026

# PN7462 auxiliary contact card slot

- ▶ The PN7462 is able to manage an auxiliary card slot, through an external contact frontend
- ▶ The auxiliary slot is supposed to be used when two or more contact cards must be accessed in the system
- ▶ The CPU and the ISO7816 UART from PN7462 are used, while the electrical management is handled by the external contact interface
- ▶ The default FW embeds a SW controlling NXP's TDA8026.



**PN7462 embedded  
Cortex M0 microcontroller**

# PN7462 memory mapping

- ▶ 40 kB **ROM** memory. It contains:
  - The primary bootloader
  - The USB mass storage primary download and the following
  - The In-Application Programming (IAP) support for flash
  - Lifecycle management of debug interface, code write protection of flash memory and USB mas storage primary download
  - USB descriptor configuration
  - Configuration of time-out and source of pad supply
- ▶ 12 kB on-chip static **RAM** memory
  - 288 Bytes reserved
- ▶ 4 kB of on-chip **EEPROM** data memory
  - 512 Bytes reserved for CLIF register constants, configuration section and NXP protected section

Reserved	0xFFFF FFFF
Private peripheral bus	0xE0FF FFFF
Reserved	0xE000 0000
APB peripheral	0x4007 FFFF
Reserved	0x4000 0000
Reserved	0x0022 AFFF
160 kB flash	0x0020 3000
Reserved	0x0020 1FFF
4 kB EEPROM	0x0020 1000
EEPROM REG	0x0020 0000
Reserved	0x0010 2FFF
12 kB SRAM	0x0010 0000
Reserved	0x0000 9FFF
40 kB ROM	0x0000 0000

# PN7462 memory mapping

- ▶ **APB peripheral** area is 512K in size
  - Divided to allow for up to 32 peripherals
  - Only peripheral from 0 to 15 are accessible
  - 16 kB of space are allocated for each peripheral, in order to simplify the address decoding for each peripheral.
- ▶ 160kB on-chip **flash** program memory programmable using ISP/IAP
  - Flash memory is divided into 2 instances of 80 kB, with each sector consisting of individual pages of 64 Bytes.
  - The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot-loader software.
  - NXP reserved 2 kB for development purposes

Reserved	0xFFFF FFFF
Private peripheral bus	0xE0FF FFFF
Reserved	0xE000 0000
APB peripheral	0x4007 FFFF
Reserved	0x4000 0000
Reserved	0x0022 AFFF
160 kB flash	0x0020 3000
Reserved	0x0020 1FFF
4 kB EEPROM	0x0020 1000
EEPROM REG	0x0020 0000
Reserved	0x0010 2FFF
12 kB SRAM	0x0010 0000
Reserved	0x0000 9FFF
40 kB ROM	0x0000 0000

# Peripherals



# PN7462 master interfaces and peripherals

## I<sup>2</sup>C master interface

- Standard I<sup>2</sup>C compliant bus interface with open-drain pins
- Standard-Mode, fast mode and fast mode plus (1 Mbps)
- Support I<sup>2</sup>C master mode only
- Programmable clocks allowing versatile rate control
- Clock stretching
- 7-bits and 10-bits I<sup>2</sup>C slave addressing
- LDM/STM instruction support
- Maximum data frame size up to 1024 bytes

## SPI master interface

- SPI master interface. Synchronous half-duplex
- Multiple data rates (1, 1.5, 2.09, 2.47, 3.01, 4.52, 5.42 and 6.78 Mbps)
- Up to two selectable salves, with selectable polarity
- Programmable clock polarity phase
- Supports 8-bit transfers
- Maximum frame size: 511 data bytes payload + 1 CRC byte
- Opt. CRC calculation (1 byte) on all data of TX and RX buffer

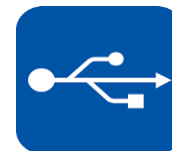
## Other peripherals

- RNG
  - 8-bit random
  - FIPS 140-2 compliant
- CRC engine
  - 16/32 bits
- Up to 21 GPIOs
  - 3.3 and 1.8V
  - Interrupts: edge or level sensitive
  - Dynamic configuration as input or output

# PN7462 host interfaces

*PN7462 offers one host interface, which can be configured in one of the following interfaces*

- ▶ HSUART for serial communication, supporting standards speeds from 9600 to 115200 bds, and faster speed up to 1.288 Mbds
- ▶ I<sup>2</sup>C supporting fast mode (extended, up to 1 Mbit/s) with multiple address support
- ▶ SPI- half duplex and full duplex, up to 7 Mbit/s
- ▶ USB 2.0 full speed, with USB 3.0 hub connection capability



# Power management and clocks

# PN7462 power management

## Integrated DC/DC and LDOs that enables:

- ▶ Class A contact cards starting 3V
- ▶ Class B and C contact cards starting 2.7V
- ▶ All features supported with a 3V power supply, including Class A smartcards

## Integrated PVDD LDO:

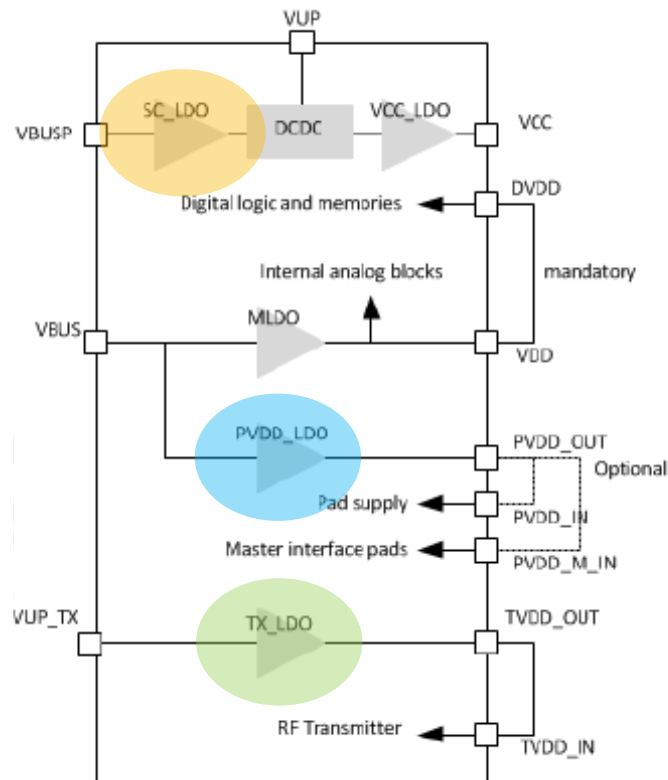
- ▶ No need of additional regulators when the power supply is 5V
- ▶ Up to 30mA

## Integrated TXLDO for stable RF power:

- ▶ Up to 180mA

## Voltage monitoring:

- ▶ Detects if the voltage is within the operational conditions to enable a proper operation of the RF interface, or the contact interface.
- ▶ VBUS (2 voltage monitors), VBUS\_P (1 voltage monitor).



# PN7462 low power modes supported

## Hard Power Down mode

- Lowest power mode; highest reduction of power consumption
- All clocks are turned off, almost all LDOs are turned off; MLDO set to low power mode

## Standby mode

- Only a small part of the digital and analog is active
- MLDO is set low power mode
- Wake-up sources are powered
- PVDDL\_LDO can be put into active mode, low power mode (default) or shut down mode
- IC wakes up from Standby in case of external activity on any communication interface

## USB suspend mode

- Only a few parts of USB are still active but not clocked
- All clock sources except LFO are stopped
- IC goes into suspend state if there is no activity on the USB bus for more than 3ms
- IC wakes up in case of new USB activity occurring on the USB Hub or on any other external activity (except Master interface).

## Active

- All functionalities are available



# PN7462 low power card detection

- ▶ The most important parameters influencing the average current consumption are:
  - Current consumption during the standby time
  - Duration of the RF polling interval
- ▶ The duration of the RF pulse needs to be long enough to properly detect any card, but it should not be too long, since it increases the average current consumption.
- ▶ The low power card detection provides a functionality which allows to power down the reader for a certain period of time to save energy

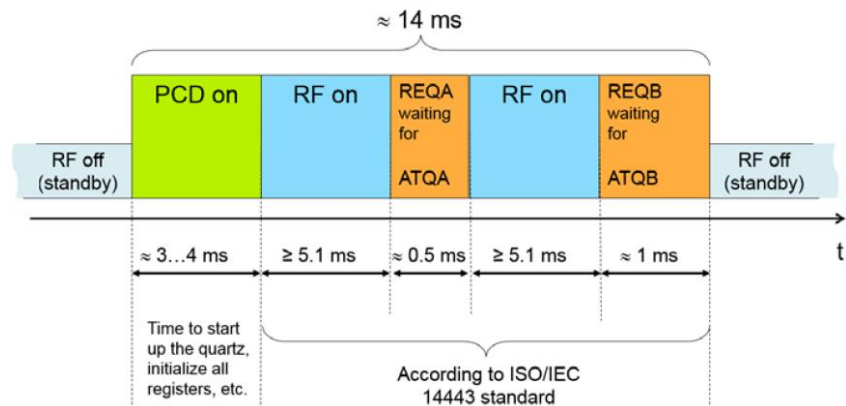


Fig 1. PCD card polling timing according to ISO/IEC14443

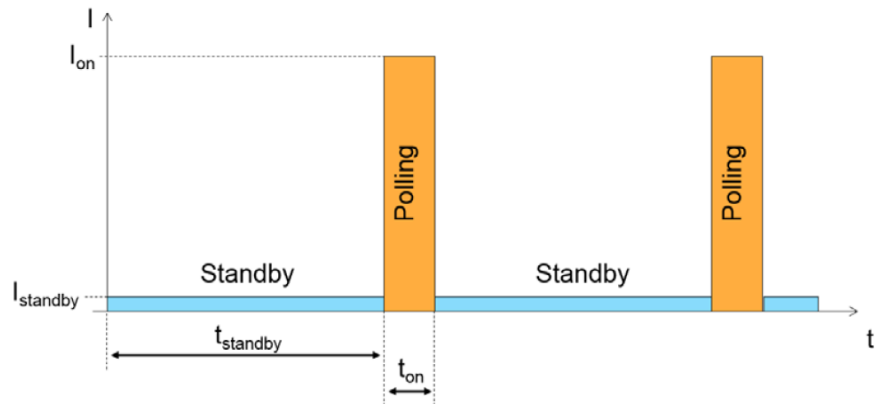


Fig 2. LPCD principle

# PN7462 primary clock sources

- ▶ **HFO (20 MHz): internal oscillator** (+/- 10% accuracy)
  - System clock source
- ▶ **LFO (365KHz): internal oscillator** (+/- 10% accuracy)
  - Clock source for always on domain of PCR
  - EEPROM clock source
  - Timers clock source
- ▶ **XTAL Osc (27.12MHz): external Xtal**
  - Reference clock for USB PLL
  - Reference clock for Int PLL
  - Clock for PageFlash
  - System clock source
  - Clock source for HSUART, I2CM, SPIM, CTIF and CLIF
- ▶ **USB clock (48 MHz): internal PLL**
  - USB IP clock
  - Div/2 clock: system clock source

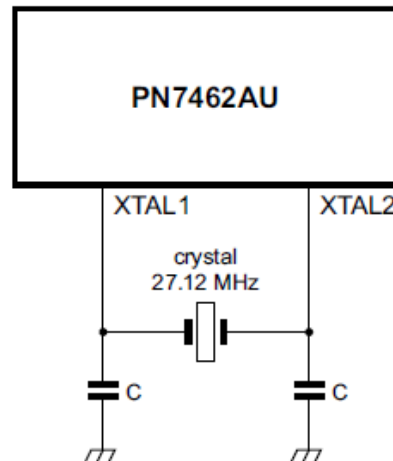


Fig 1. Crystal oscillator connection

**PN7462**

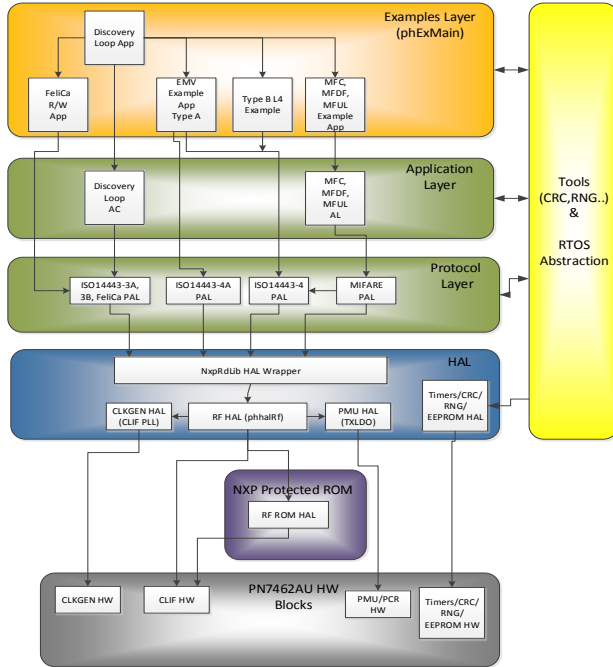
**Product support package**



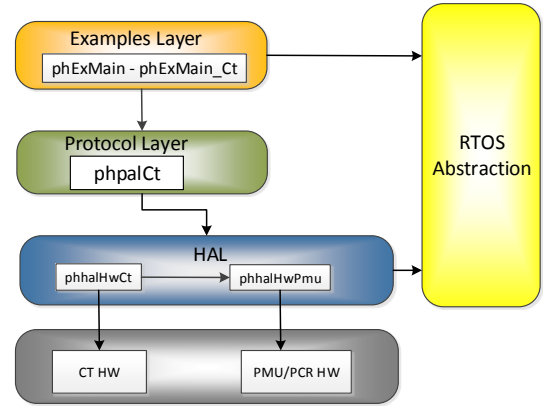


# PN7462 full software development package

Contactless interface



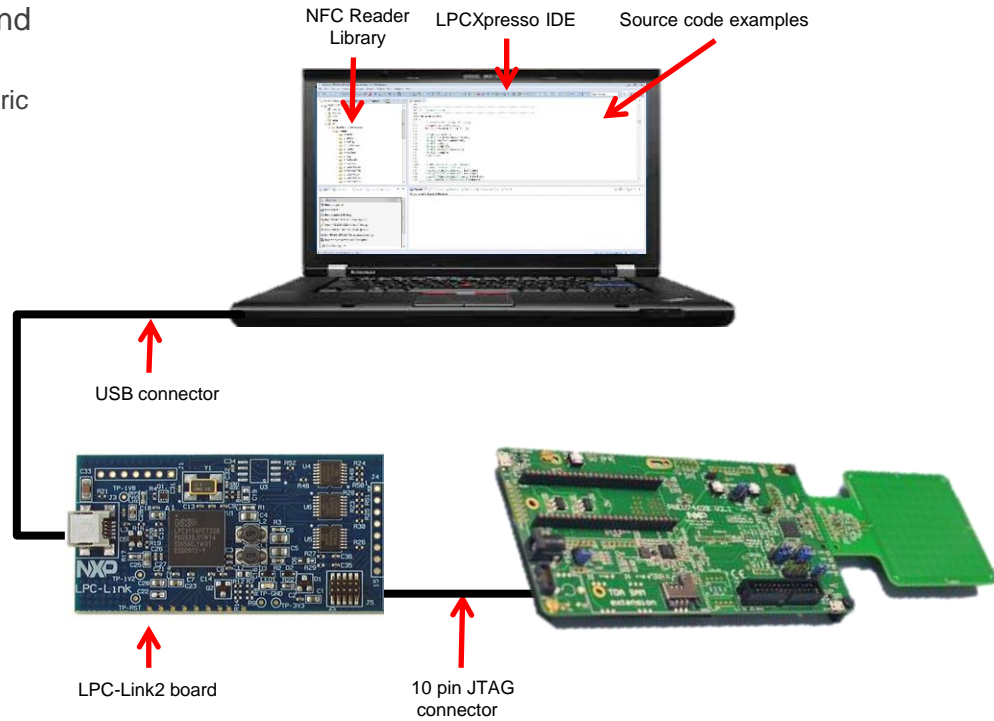
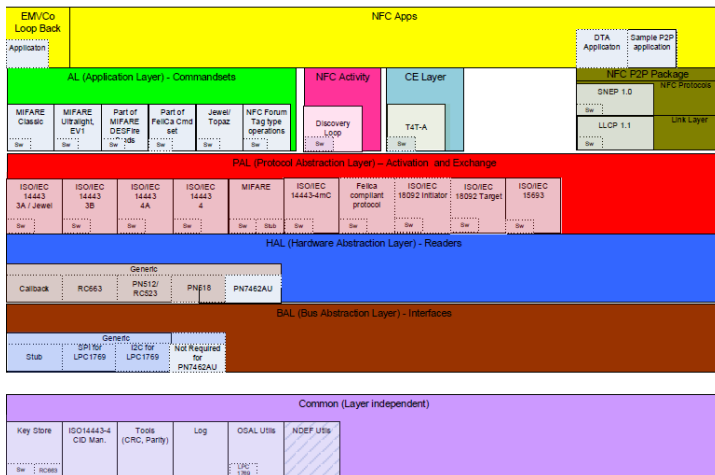
Contact interface



- Customer application or examples
- Reader Library
- HAL
- PN7462 HW

# Easy test and debugging based on NFC Reader Library examples

- ▶ The NFC Reader Library is encapsulated into layers and components written in ANSI C.
  - Each layer consists of different components having a generic interface and a specific implementation
- ▶ The library structure provides a modular way of programming and setting up the reader interface.



# PN7462 NFC Cockpit, the complete design tool for engineers

- ▶ The NFC Cockpit is a PC based interface which allows to easy control all PN7462 functions.
- ▶ The support tool is composed of these parts:
  - Registers and EEPROM access
  - Low Power Card Detect(LPCD)
  - Dynamic Power Control(DPC)
  - Test signals control
  - Generic commands
  - Log monitor
  - Type cards
  - Status bar

PN7462AU NFC Cockpit v1.3.0.0

Operation  
 EEPROM  Register

Register address: 0h  
Read Write

Bit selection:  
Binary  
Hex Value: 0h

Write Operation  
 All bits  
 Single bit

Registers/EEPROM access

Single Byte EEPROM Access  
Address: 0x00000000 Read EEPROM  
Data: 0x00 Write EEPROM  
Select XML folder XML -> BIN  
BIN -> XML Dump EEPROM

RF Field Control  
Field ON Field OFF RF Reset

Test Signal Control  
Analog GPIO1: Analog GPIO2:  
Route Analog Signal  
Digital GPIO4: Digital GPIO5:  
Route Digital Signal

Log Monitor

Type Cards: DPC RF Power LPCD  
Type A Type B Type F ISO15693

Protocol Layer  
Layer 14443-3a  
Activate Layer3 Halt 106 kBd/s Load Protocol  
ATO: 0h Last SAK: 0h Re-Activate L3  
UID: 0h Perform Single/Endless REQA  
 Single REQA  Endless REQA  
Inter-REQ: ms  
 RFRESET  
Time-out RFON: ms  
Single REQA

Layer 14443-4a  
Select a baud rate: 106 kBd/s  
Activate Layer4 Deselect Card  
ATS: 0h

Layer 14443-4: Data Exchange with PICC  
Data to be send: 0h  
 TXCRC Enable  RXCRC Enable Send Data  
Card response: 0h

Application Layer  
Command GetAppIds MF DesFire  
GetAppIds  
Applications on the card:

Status:  Help Save log

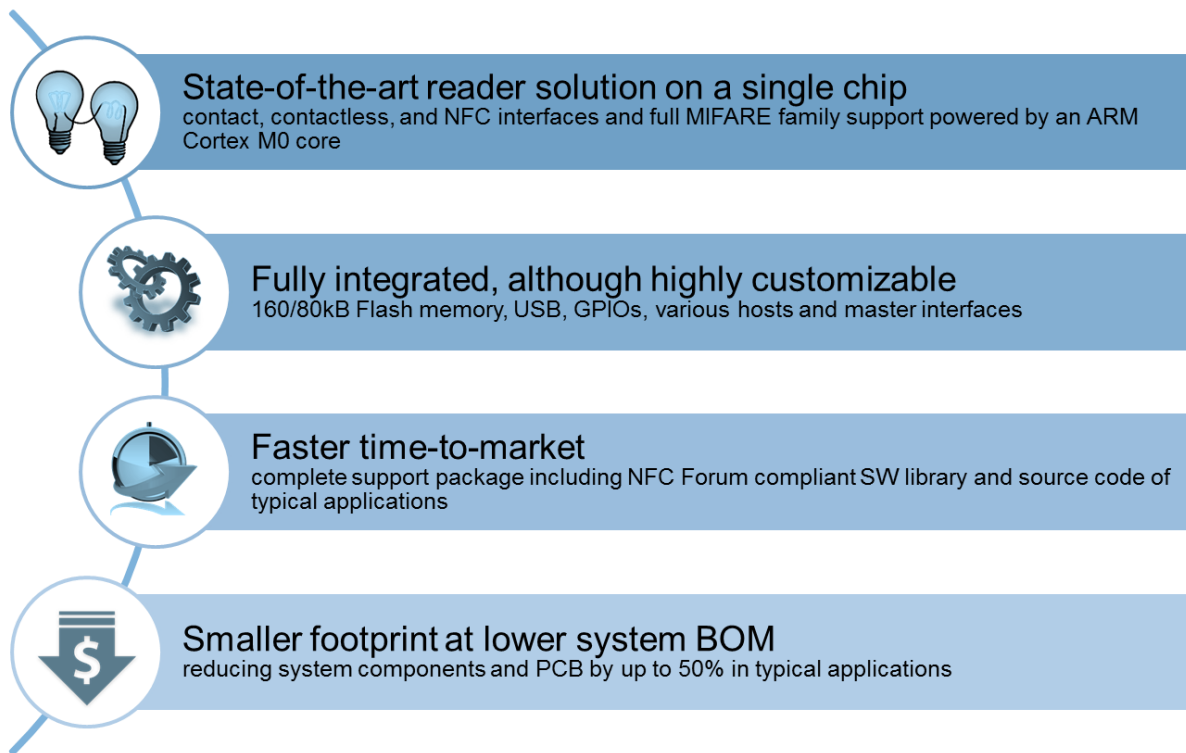
Board not connected

# PN7462 product documentation

Doc ID	Doc Name	Description
PN746x_736X	NFC Cortex-M0 microcontroller with ISO/IEC7816 interface	This document describes the functionality and electrical specification of the PN7462 NFC controller family
AN11706	PN7462AU Antenna design guide	This document describes the antenna design related to the PN7462AU
AN11738	PN7462AU Contact smart card application	This document describes how to use the contact smart card interface on the PN7462AU
AN11784	PN7462AU How to integrate RTOS	This document describes the steps required for integration of RTOS with PN7462AU firmware
AN11785	PN7462AU LPCD and standby mode	This document describes the principle of low power card detection offered by the PN7462AU
UM10833	PN7462 Quick Start Guide - customer board	This document describes the required basic circuitry to operate the PN7462AU and it also describes how to setup and use the PN7462AU customer demo board
UM10913	Software User Manual	This document describes the PN7462AU/PN7360AU FW architecture and how to use it
UM10957	PN7462AU door access user manual	This document server as a user manual for the Door Access Demo application use case demo on PN7462 board
UM10915	PN7462AU PC CCID reader user manual	This document briefs the setup environment required for PC CCID reader use case demo on PN7462 board
UM10951	PN7462 Reference POS application	This document briefs the setup environment required for the POS application use case demo on PN7462 board

**Final remarks**

# PN7462 - first all-in-one full NFC solution



# PN7462 family ordering information and samples



Product	Flash memory	Contact interface	Delivery	12NC
PN7462	160 kB	Yes	Single Tray	9353 076 92551
			Reel	9353 076 92518
PN7362	160 kB	No	Single Tray	9353 084 36551
			Reel	9353 084 36518
PN7362	80 kB	No	Single Tray	9353 077 96551
			Reel	9353 077 96518

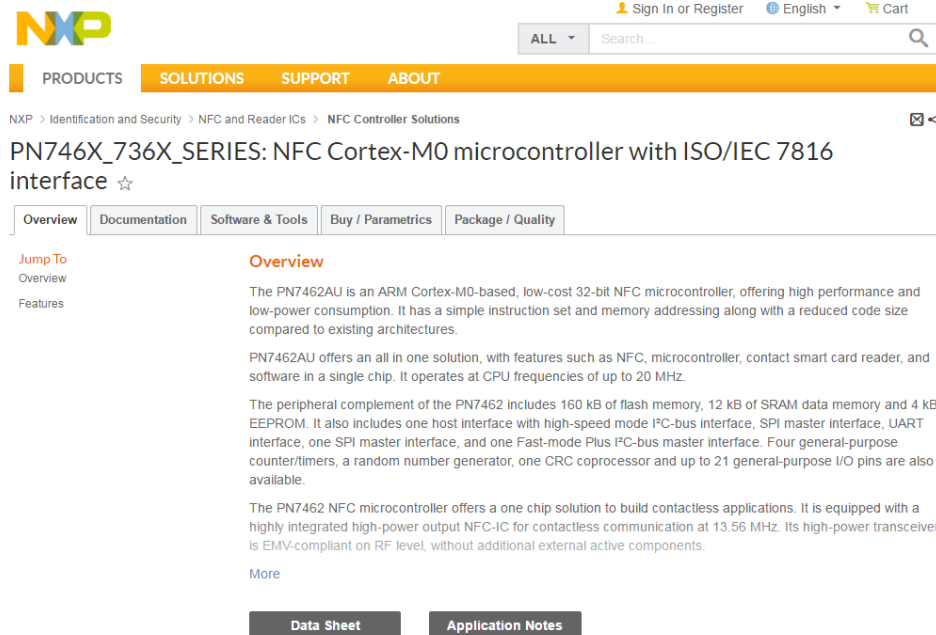
Product samples can be ordered from eSample by clicking on “NXP Customer Support” → “Samples” or distributors



# Do you need more?

## Resources and useful links

- ▶ NFC Everywhere  
<http://www.nxp.com/nfc>
- ▶ PN7462 family product website  
[http://www.nxp.com/products/identification-and-security/nfc-and-reader-ics/nfc-controller-solutions/nfc-cortex-m0-microcontroller-with-iso-iec-7816-interface:PN746X\\_736X\\_SERIES](http://www.nxp.com/products/identification-and-security/nfc-and-reader-ics/nfc-controller-solutions/nfc-cortex-m0-microcontroller-with-iso-iec-7816-interface:PN746X_736X_SERIES)
- ▶ OM27462CDK NFC controller development kit website  
<http://www.nxp.com/products/identification-and-security/nfc-and-reader-ics/nfc-controller-solutions/nfc-controller-development-kit:OM27462CDK>
- ▶ NFC support community  
<https://community.freescale.com/community/nfc?hdr=1&subcf=SUPPORT>



The screenshot shows the NXP website product page for the PN746X\_736X\_SERIES. The page features a navigation bar with 'PRODUCTS', 'SOLUTIONS', 'SUPPORT', and 'ABOUT'. The breadcrumb trail is 'NXP > Identification and Security > NFC and Reader ICs > NFC Controller Solutions'. The product title is 'PN746X\_736X\_SERIES: NFC Cortex-M0 microcontroller with ISO/IEC 7816 interface'. Below the title are tabs for 'Overview', 'Documentation', 'Software & Tools', 'Buy / Parameters', and 'Package / Quality'. The 'Overview' tab is selected, showing a description of the PN7462AU as an ARM Cortex-M0-based, low-cost 32-bit NFC microcontroller. It also mentions the PN7462AU as a single-chip solution and lists peripheral features like 160 kB of flash memory, 12 kB of SRAM, and 4 kB of EEPROM. A 'More' link is visible at the bottom of the overview section. At the bottom of the page, there are buttons for 'Data Sheet' and 'Application Notes'.



**Software development** in Android and iOS

**Embedded software** for MCUs

**JCOP, Java Card** operating Systems

**Hardware design and development**

Digital, analog, sensor acquisition, power management

**Wireless communications** WiFi, ZigBee, Bluetooth, BLE

**Contactless antenna** RF design, evaluation and testing

**MIFARE** applications

End-to-end systems, readers and card-related designs

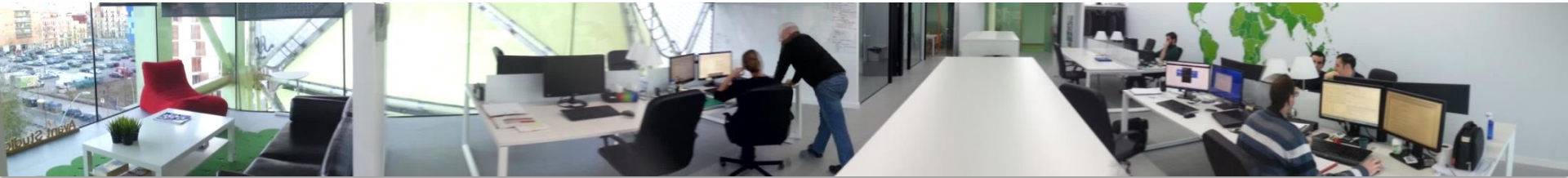
**EMVco** applications

Readers, cards, design for test compliancy (including PCI)

**Secure Element management**

GlobalPlatform compliant backend solutions

**Secure services provisioning** OTA, TSM services



We help companies leverage the  
mobile and contactless revolution



**MobileKnowledge**  
Roc Boronat 117, P3M3  
08018 Barcelona  
(Spain)

Get in touch with us  
[www.themobileknowledge.com](http://www.themobileknowledge.com)  
[mk@themobileknowledge.com](mailto:mk@themobileknowledge.com)



# PN7462 family - first all-in-one full NFC solution

Jordi Jofre (Speaker) / Eric Leroux (Host)

## Thank you for your kind attention!

- ▶ Please remember to fill out our [evaluation survey](#) (pop-up)
- ▶ Check your email for [material download](#) and on-demand [video](#) addresses
- ▶ Please check NXP and MobileKnowledge websites for [upcoming webinars](#) and [training sessions](#)

<http://www.nxp.com/support/classroom-training-events:CLASSROOM-TRAINING-EVENTS>

[www.themobileknowledge.com/content/knowledge-catalog-0](http://www.themobileknowledge.com/content/knowledge-catalog-0)



**Thank you**