



NTAG I²C plus – Your entryway to NFC

Product support package

Public
MobileKnowledge
March 2016

Agenda

Session 9th March: *NTAG I²C plus – Your entryway to NFC*

- ▶ *Introduction, use cases, target markets and benefits*
- ▶ *Positioning and NTAG portfolio*
- ▶ *Memory map*
- ▶ *Key functionalities*
- ▶ *Demokit and PSP quick overview*
- ▶ *Ordering details and wrap up*

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Session 16th March: *NTAG I²C plus – Product Support Package*

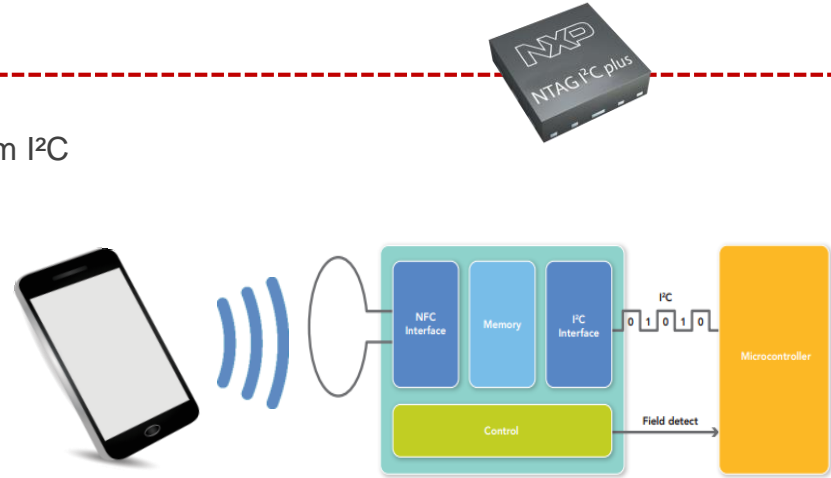
- ▶ Where to find NTAG I²C *plus* documentation
- ▶ NTAG I²C *plus* Demo Kit
- ▶ How to evaluate NTAG I²C *plus*
- ▶ How to develop applications around NTAG I²C *plus* from I²C and RF sides



NTAG I²C *plus* is the simplest, most cost-effective NFC solution

The simplest, most cost-effective NFC solution

- Easy access to data from both RF (Type 2 tag) and from I²C
- Field detection to wake up connected devices
- Energy Harvesting capabilities
- EEPROM for offline data access
- Maximum interoperability with NFC devices
- Flexible memory management
- Originality signature for protection against cloning
- Fast & convenient data exchange via a 64 bytes SRAM buffer
- Small footprint package (1,6*1,6*0,5mm)



NTAG I²C *plus* key features

Field detection



- Configurable field-detection output signal for data transfer synchronization and device wake up

Energy harvesting



- Energy harvesting from the NFC field to power external devices

SRAM memory



- 64 bytes SRAM volatile memory without write endurance limitation

SRAM mirroring



- Mapping the SRAM memory into the user memory

Pass through mode



- For fast data exchange of large files via the SRAM buffer

Originality signature



- Originality signature based on ECC for simple genuine authentication

NFC silence mode



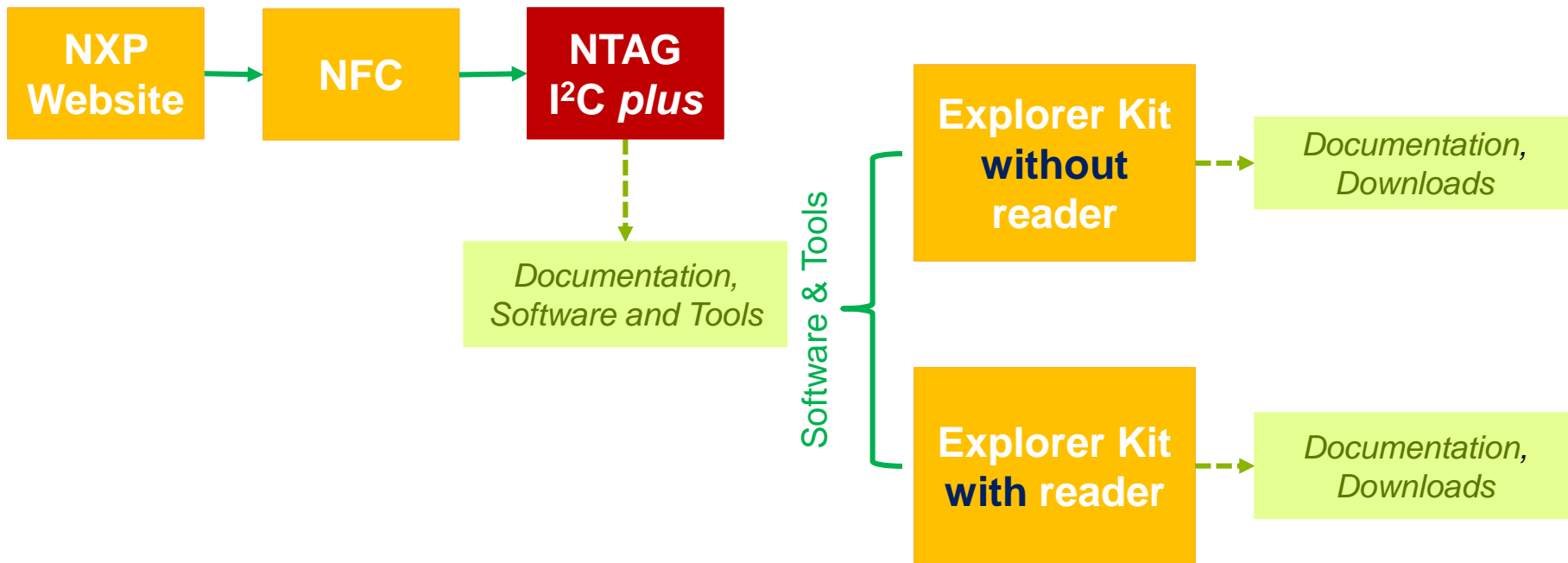
- NFC silence to disable NFC interface

Memory access management



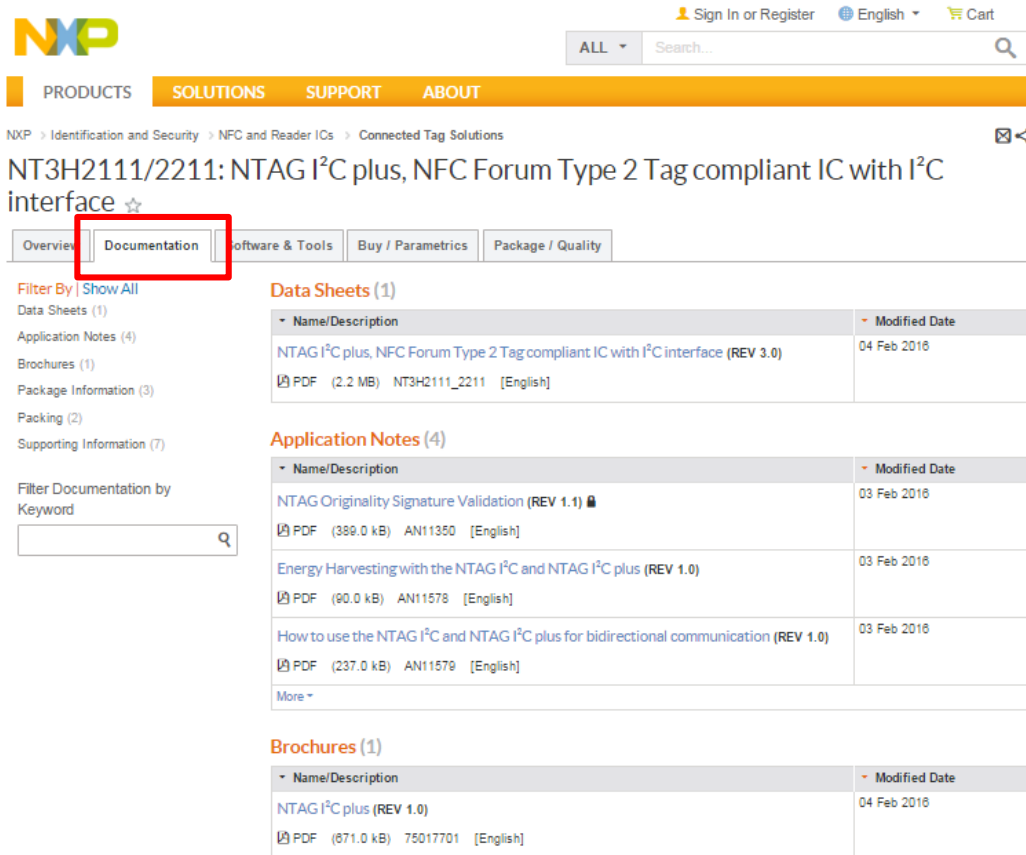
- Memory access configuration from both the NFC and I²C interfaces.

Where to find NTAG I²C *plus* documentation



Where to find NTAG I²C *plus* documentation

NTAG I²C *plus* site




The screenshot shows the NXP website interface for the NTAG I²C *plus* product. The top navigation bar includes links for Sign In or Register, English, and Cart. The main navigation bar has tabs for PRODUCTS, SOLUTIONS, SUPPORT, and ABOUT. The breadcrumb trail indicates the path: NXP > Identification and Security > NFC and Reader ICs > Connected Tag Solutions. The product title is "NT3H2111/2211: NTAG I²C *plus*, NFC Forum Type 2 Tag compliant IC with I²C interface". Below the title, there are tabs for Overview, Documentation (highlighted with a red box), Software & Tools, Buy / Parameters, and Package / Quality. The left sidebar shows a list of document types: Data Sheets (1), Application Notes (4), Brochures (1), Package Information (3), Packing (2), and Supporting Information (7). The main content area displays three sections: Data Sheets (1), Application Notes (4), and Brochures (1). Each section contains a table with columns for Name/Description and Modified Date.

Data Sheets (1)

Name/Description	Modified Date
NTAG I ² C <i>plus</i> , NFC Forum Type 2 Tag compliant IC with I ² C interface (REV 3.0) PDF (2.2 MB) NT3H2111_2211 [English]	04 Feb 2016

Application Notes (4)

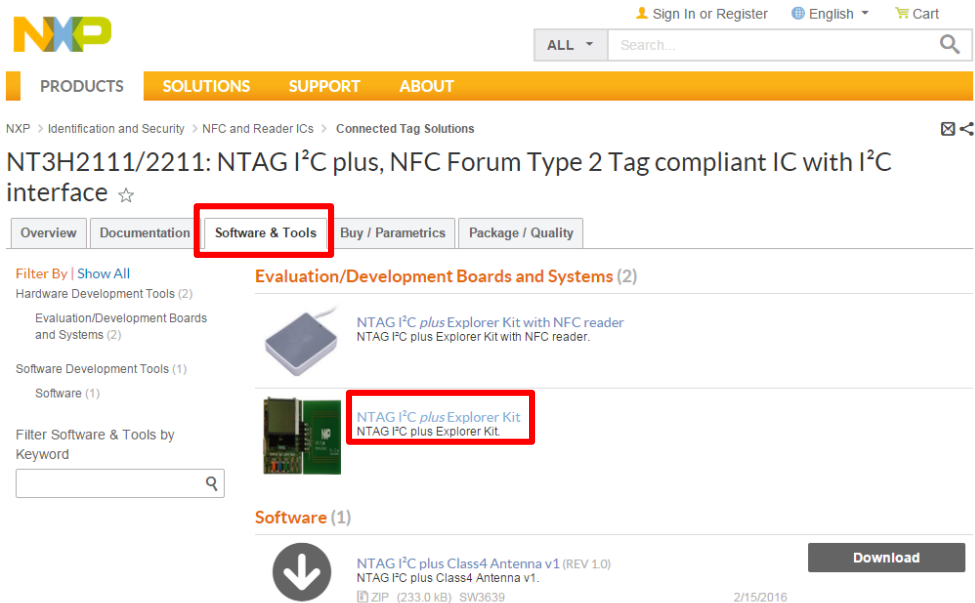
Name/Description	Modified Date
NTAG Originality Signature Validation (REV 1.1)  PDF (389.0 kB) AN11350 [English]	03 Feb 2016
Energy Harvesting with the NTAG I ² C and NTAG I ² C <i>plus</i> (REV 1.0) PDF (60.0 kB) AN11578 [English]	03 Feb 2016
How to use the NTAG I ² C and NTAG I ² C <i>plus</i> for bidirectional communication (REV 1.0) PDF (237.0 kB) AN11579 [English]	03 Feb 2016
More	

Brochures (1)

Name/Description	Modified Date
NTAG I ² C <i>plus</i> (REV 1.0) PDF (671.0 kB) 75017701 [English]	04 Feb 2016

Where to find NTAG I²C *plus* documentation

NTAG I²C *plus* site



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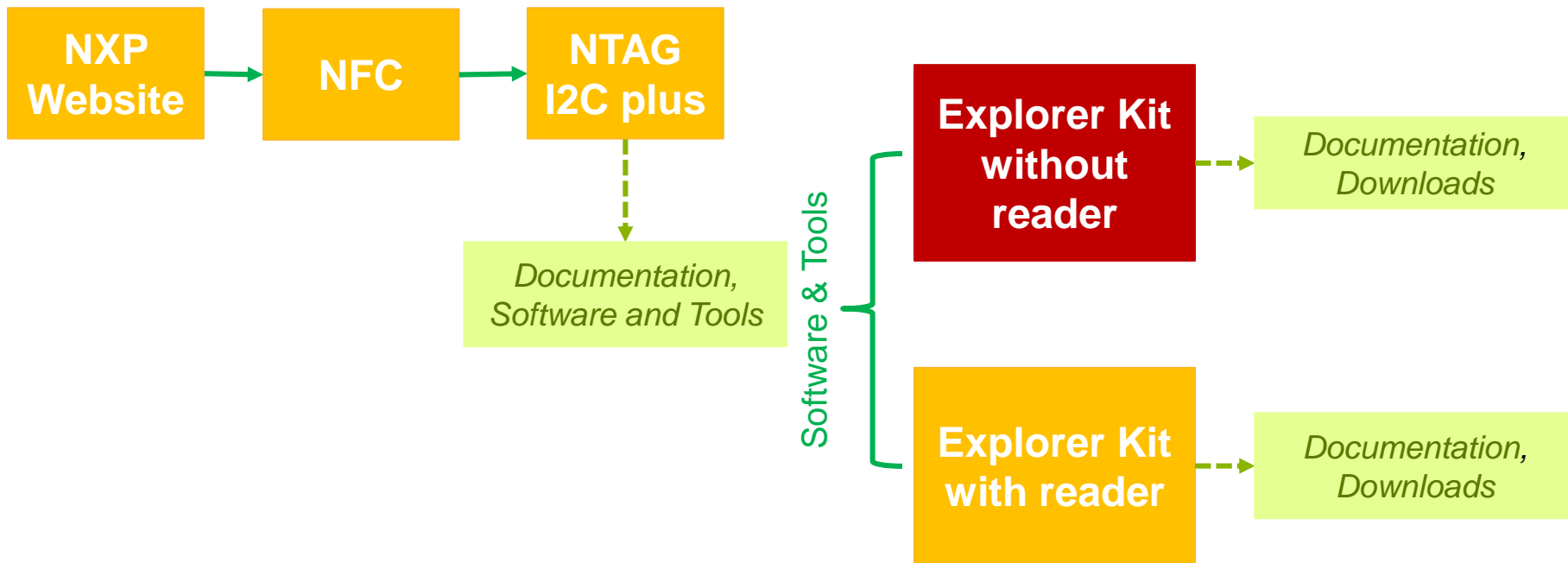
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NTAG I²C <i>plus</i> Explorer Kit and Android Demo (REV 1.0)	23 Feb 2016
PDF (1.5 MB) UM10966 [English]	
NTAG I²C <i>plus</i> Explorer Kit Program and Debug Start-up (REV 1.0)	17 Feb 2016
PDF (436.0 kB) UM10945 [English]	

Supporting Information (1)

Name/Description	Modified Date
NTAG Antenna Design Guide (REV 1.4)	24 Feb 2016
ZIP (4.8 MB) AN11276 [English]	

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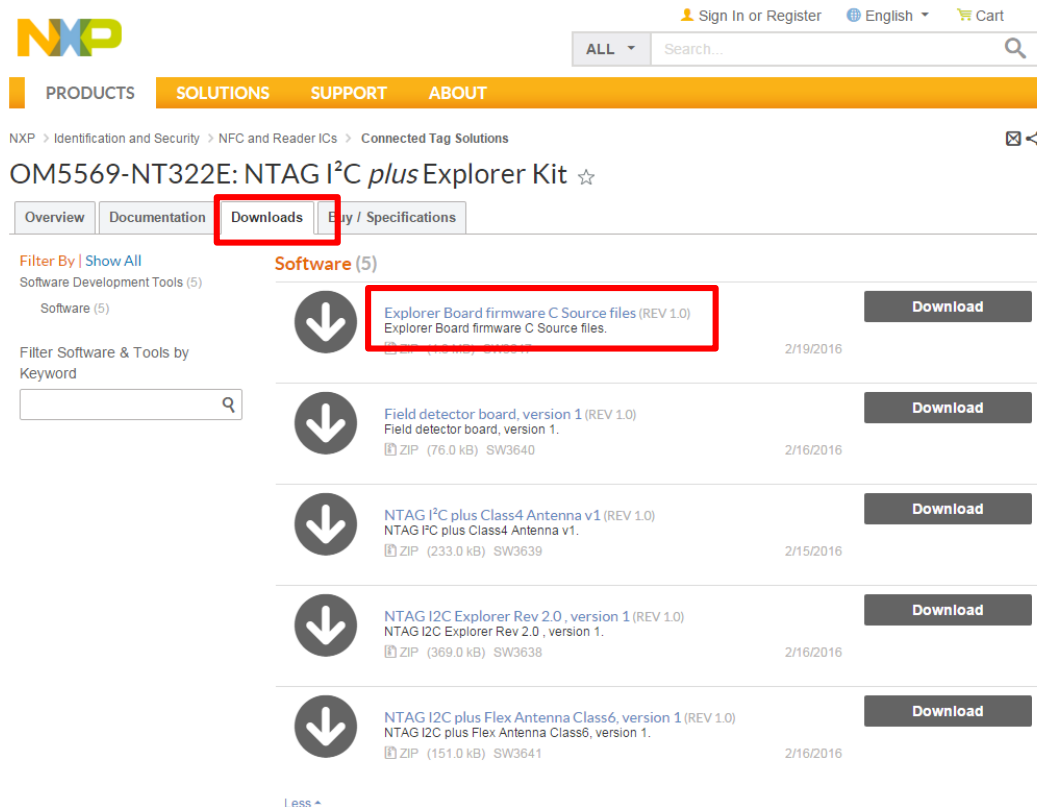
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Software (5)

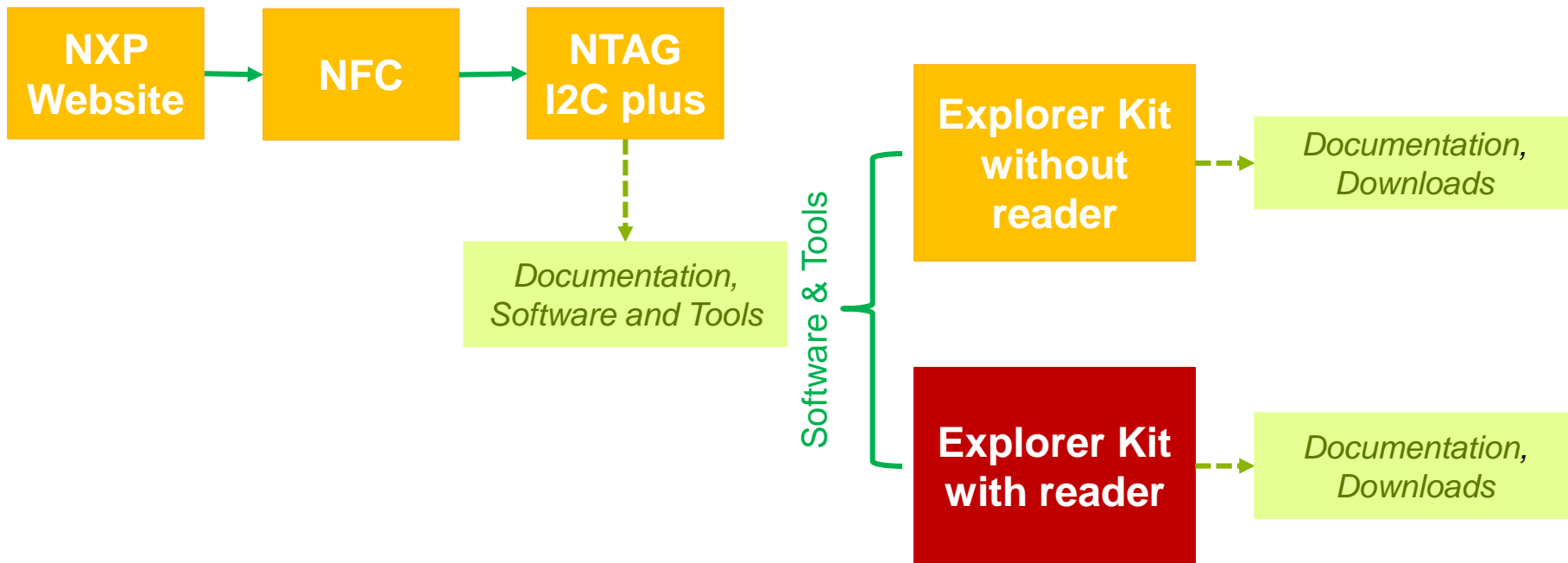
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Setup of PC Windows application for use with Identiv Reader (REV 1.0)
Setup of PC Windows application for use with Identiv Reader.

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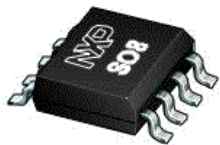
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NTAG I²C *plus*

Demo Kit

NTAG I²C *plus* Demo Kit



Demokit	NTAG I ² C plus Demo Kit
Firmware	SW3647 – Explorer Board firmware C Source files
Peek and Poke	SW3652 – Peek & Poke
Android Application	https://play.google.com/store/apps/details?id=com.nxp.ntagi2cdemo&hl=de
Windows Application	SW3651 - Setup of PC Windows application for use with Identiv Reader
Documentation	NT3H2111/NT3H2211 NTAG I²C plus - Product datasheet AN11578 - Energy Harvesting with the NTAG I ² C and NTAG I ² C plus AN11579 - How to use the NTAG I ² C and NTAG I ² C plus for bi-directional NTAG I ² C plus AN11350 - NTAG Originality Signature Validation AN11276 - Antenna design guide AN11786 - NTAG I ² C <i>plus</i> memory configuration options UM3587 - NTAG I ² C Explorer Peek and Poke GUI UM3587 - NTAG I ² C Explorer Demo app UM10945 - NTAG I ² C plus Explorer Kit Program and Debug Start-up UM10966 - NTAG I ² C plus Explorer Kit and Android Demo

NTAG I²C *plus* Demo Kit

OM5569/NT322E includes:

- ▶ Explorer Board
- ▶ NXP NT3H2211 NTAG I²C *plus*
- ▶ Field detector board
- ▶ 10 NTAG I²C *plus* samples
- ▶ Flex antenna

OM5569/NT322ER includes an external USB reader

OM5569/NT322F includes an additional set of flex antennas



NTAG I²C *plus* Demo Kit

About the Explorer Board:

- ▶ 5 buttons (3 Color buttons, RESET and ISP)
- ▶ NXP LM75B digital temperature sensor
- ▶ NXP LPC1114 32-bit ARM Cortex-M0 microcontroller
- ▶ thermal watchdog
- ▶ RGB light
- ▶ LCD display
- ▶ microUSB for PC connection
- ▶ JTAG for FW upload
- ▶ I2C Bus Connector



NTAG I²C *plus*

How to evaluate

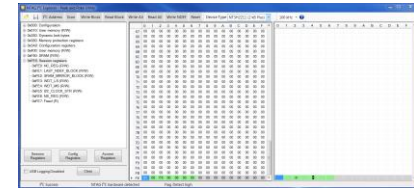
Software Tools to evaluate NTAG I²C *plus*

Explorer
Demo kit
Applications

Android Application

Pc Windows Application

Peek and Poke



Software Tools to evaluate NTAG I²C *plus*

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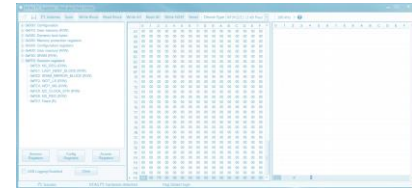
Android Application



Pc Windows Application

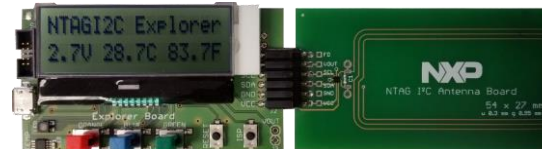
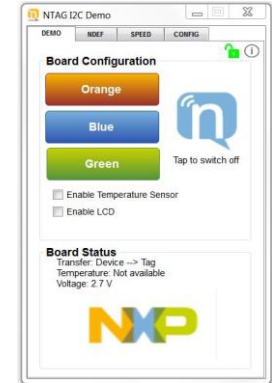


Peek and Poke



NTAG I²C *plus* Explorer Kit Demo Application

- ▶ The functionalities of the Android and Windows application are the same.
- ▶ Shows the I²C bi-directional communication.
- ▶ Read/Write NDEF to EEPROM.
- ▶ Speed tests of the SRAM and EEPROM communication.
- ▶ Read/Write registers.
- ▶ Read all memory.
- ▶ Upload new firmware.



NTAG I²C *plus* Explorer Kit Demo Application

Led Demo Tab



NTAG I²C *plus* Explorer Kit Demo Application

NDEF Tab



NTAG I²C *plus* Explorer Kit Demo Application

Speed Tab

There are two types of tests

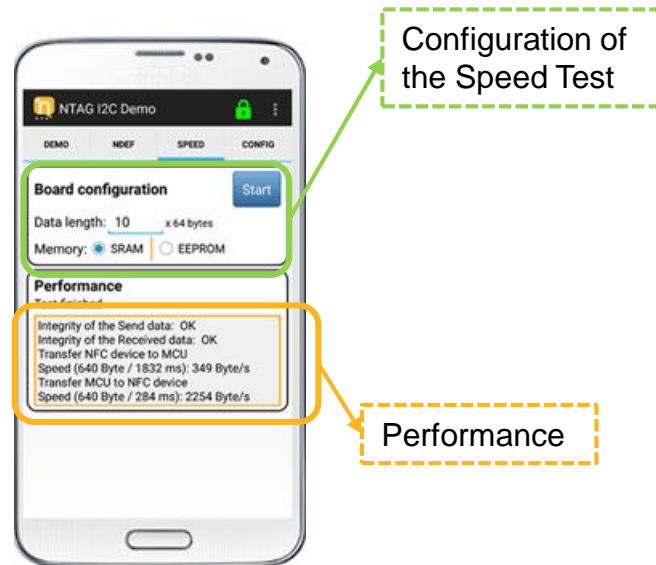
- ▶ SRAM Test
- ▶ EEPROM Test

SRAM Tests

- ▶ Measure the data transfer speed from/to the application to/from the microcontroller through the SRAM.
- ▶ The application writes data to the SRAM several times, and the microcontroller reads from it.
- ▶ NTAG I²C PLUS in Pass-Through mode

EEPROM Tests

- ▶ It measures the speed at which the application is able to write and read the EEPROM memory of the NTAG I²C PLUS.
- ▶ An NDEF message is written to the EEPROM, and then, the same NDEF message is read.



NTAG I²C *plus* Explorer Kit Demo Application

Config Tab

Read Tag Memory

- ▶ It shows the whole memory of the NTAG I²C PLUS product.
- ▶ The pages from 0xE2h to 0xFFh in the sector 0 are hidden for security reasons (PWD, PACK, AUTH0, PT_I2C and ACCESS bytes).

Read Tag Memory

Reset Tag

- ▶ It sets the original content programmed by production.
- ▶ The access configuration is also set to default: PWD to 0xFFFFFFFF, AUTH0 to 0xFF, PACK to 0x0000, ACCESS to 0x00 and PT_I2C to 0x00.

Reset Tag

Read Session Registers

- ▶ It shows the value of the session registers. They are read only from NFC interface.

Read Session Registers

Read/Write Config Registers

Read/Write Config Registers

- ▶ It shows the configuration registers and allows the user to write them.



NTAG I²C *plus* Explorer Kit Demo Application

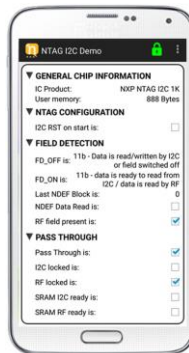
Config Tab



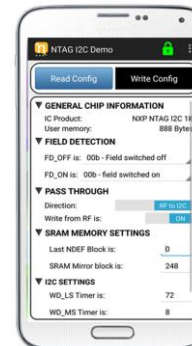
Read Tag
Memory



Reset Tag



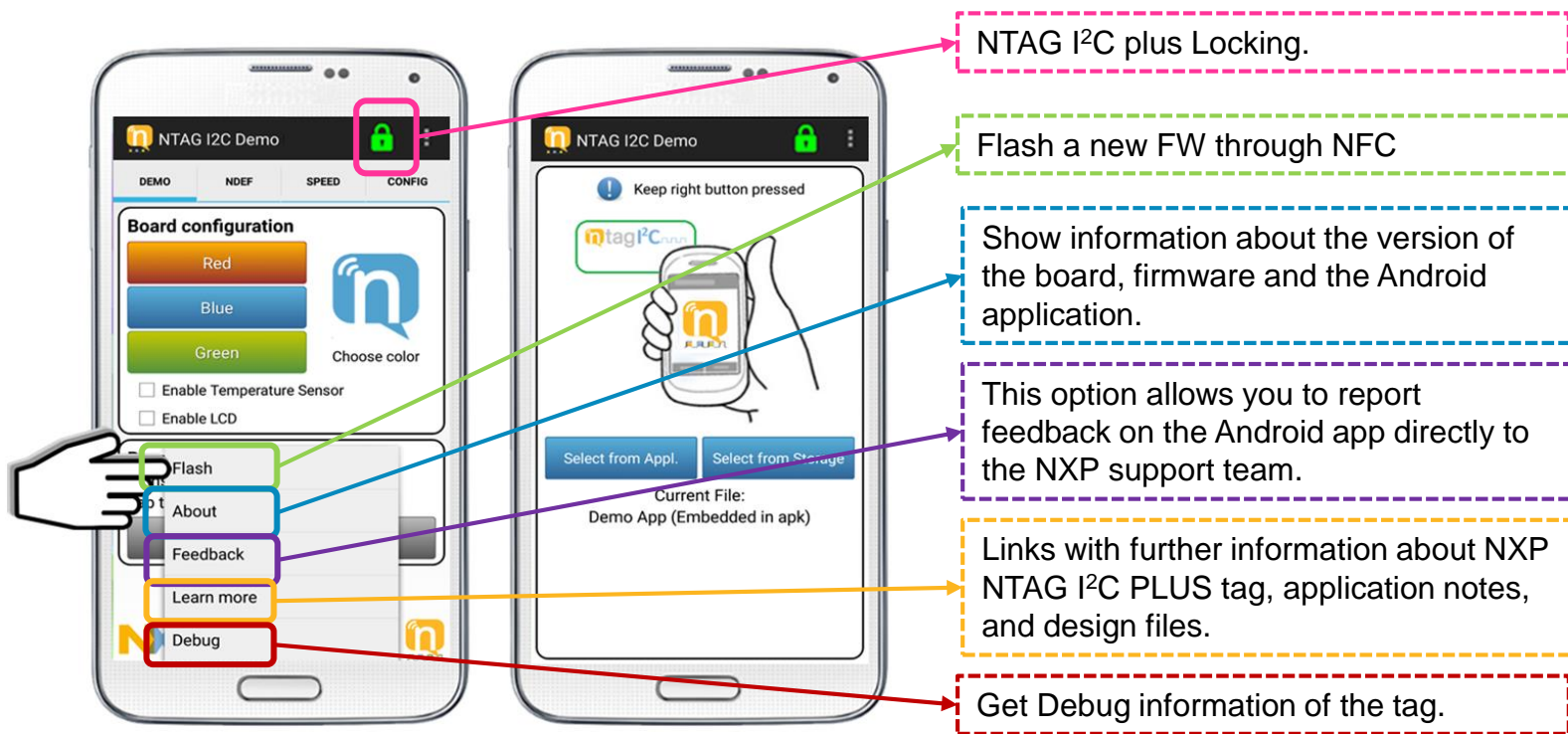
Read Session
Registers



Read/Write
Config Registers

NTAG I²C *plus* Explorer Kit Demo Application





Action Bar



NTAG I²C *plus* Explorer Kit Demo Application

Authentication

- ▶ The NTAG I²C *plus* offers authentication to protect memory operations. The device can be locked or not.
- ▶ The device status is shown on the locker icon and it can be:

Device	State	Description	Icon
NTAG I ² C	All open.	No Authentication feature.	
NTAG I ² C <i>plus</i>	Unlocked	Memory is unprotected.	
NTAG I ² C <i>plus</i>	Locked and not authenticated	Memory is protected and user has not introduced the correct password. No Access.	
NTAG I ² C <i>plus</i>	Locked and authenticated.	Memory is protected and user has introduced the correct password.	

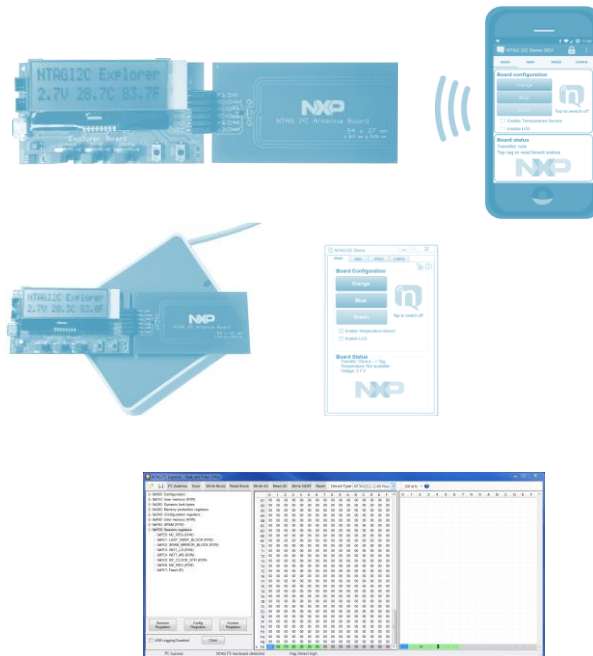
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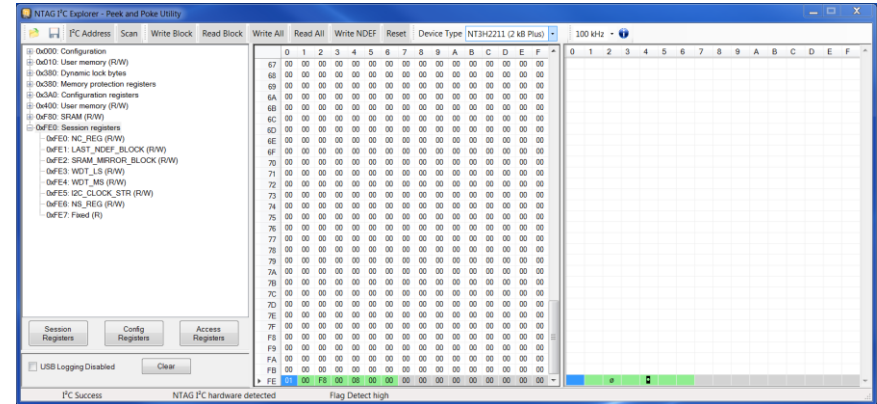
Pc Windows Application

Peek and Poke



NTAG I²C *plus* Peek and Poke

- ▶ PC-based tool working via I²C serial bus interface.
- ▶ Exploration of detailed memory content of the EEPROM.
- ▶ Read/Write all memory.
- ▶ Read/Write a block of memory.
- ▶ Read/Write NDEF messages.
- ▶ Read/Write Access, Session and Configuration registers.
- ▶ Read/Write I²C address.



NTAG I2C *plus* Peek and Poke

Action Bar

Export/Import
Memory
Contents

Scan all I2C
Address

Change I2C Address
of the NTAG I2C *plus*

The screenshot displays the NTAG I2C Explorer - Peek and Poke Utility interface. The top window shows a memory scan of the NT3H1101 (1 kB) device at 100 kHz. The left pane lists memory addresses from 0x010 to 0x160, categorized as User memory (R/W). The main pane shows a hex dump of the memory contents, with the first few rows highlighted in green. A dialog box titled "I2C device found at address 0xAA" is displayed over the hex dump.

The bottom window shows the same utility for the NT3H2211 (2 kB Plus) device at 100 kHz. The left pane lists memory addresses from 0x000 to 0x0F0, categorized as Configuration and User memory (R/W). The main pane shows a hex dump of the memory contents, with the first few rows highlighted in blue. A dialog box titled "Edit I2C Address" is displayed over the hex dump, showing the current I2C address as 0xAA and a new I2C address field.

Annotations with pink dashed boxes and arrows highlight specific features:

- Export/Import Memory Contents:** Points to the file icon in the top-left corner of the NTAG I2C Explorer - Peek and Poke Utility window.
- Scan all I2C Address:** Points to the "Scan" button in the top-left corner of the NTAG I2C Explorer - Peek and Poke Utility window.
- Change I2C Address of the NTAG I2C *plus*:** Points to the "Edit I2C Address" dialog box in the bottom window.

NTAG I2C *plus* Peek and Poke

Action Bar

Read/Write Block Controls

0x000: Configuration
0x000: PC address (R/W)
0x001: Serial Number
0x007: Internal device ID
0x00A: Lock byte
0x00C: Capability
0x010: User memory (R/W)
0x010: User memory (R/W)
0x020: User memory (R/W)
0x030: User memory (R/W)
0x040: User memory (R/W)
0x050: User memory (R/W)
0x060: User memory (R/W)

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	AA	00	00	00	00	00	00	00	00	00	00	E1	10	6D	00	
01	03	00	FE	00	00	00	00	00	00	00	00	00	00	00	00	
02	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
03	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
04	73	65	63	75	72	69	74	79	2F	73	6D	61	72	74	5F	6C
05	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
06	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
07	48	31	31	30	31	5F	4E	54	33	48	31	32	30	31	2E	68
08	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
09	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
0A	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	
0B	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	

Read/Write All Memory

0x000: Configuration
0x010: User memory (R/W)
0x380: Dynamic lock bytes
0x380: Memory protection registers
0x3A0: Configuration registers
0x400: User memory
0xF80: SRAM (R/W)
0xFE0: Session ID

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	04	0F	4D	42	5A	4C	80	00	44	00	00	00	E1	10	EF	00
01	03	60	91	02	36	53	70	91	01	15	54	02	65	6E	4E	54
02	41	47	20	49	C2	B2	43	20	45	58	50	4C	4F	52	45	52
03	13	01	19	55	01	6E	78	70	2E	63	6F	6D	2F	64	65	6D
04	6F	62	6F	61	72	64	2F	4F	4D	35	35	36	39	54	0F	17
05	61	6E	64	72	6F	69	64	2E	63	6F	6D	3A	70	6B	67	63
06	6F	6D	2E	6E	78	70	2E	6E	74	61	67	69	32	63	64	65
07	6D	6F	FE	00	00	00	00	00	00	00	00	00	00	00	00	00
08	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
09	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0A	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0B	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0C	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0D	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0E	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0F	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20

Action Bar

I2C Address Scan Write Block Read Block Write All Read All Write NDEF Reset Device Type NT3H2211 (2 kB Plus) 100 kHz

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	4	5	M	B	6	S	p					6	7	8	9	A
01	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
02	A	G														
03	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!
04	o	b	o	a	r	d	/	O	M	5	5	6	9	T	!	!
05	a	n	d	r	o	i	d									
06	o	m														
07	m	o														

NTAG I²C *plus* Peek and Poke

Action Bar

The screenshot displays the NTAG I²C *plus* software interface. At the top, a toolbar contains buttons for I²C Address, Scan, Write Block, Read Block, Write All, Read All, Write NDEF (highlighted with a blue box), and Reset. To the right of these buttons, the Device Type is set to NT3H2211 (2 kB Plus) and the frequency is 100 kHz.

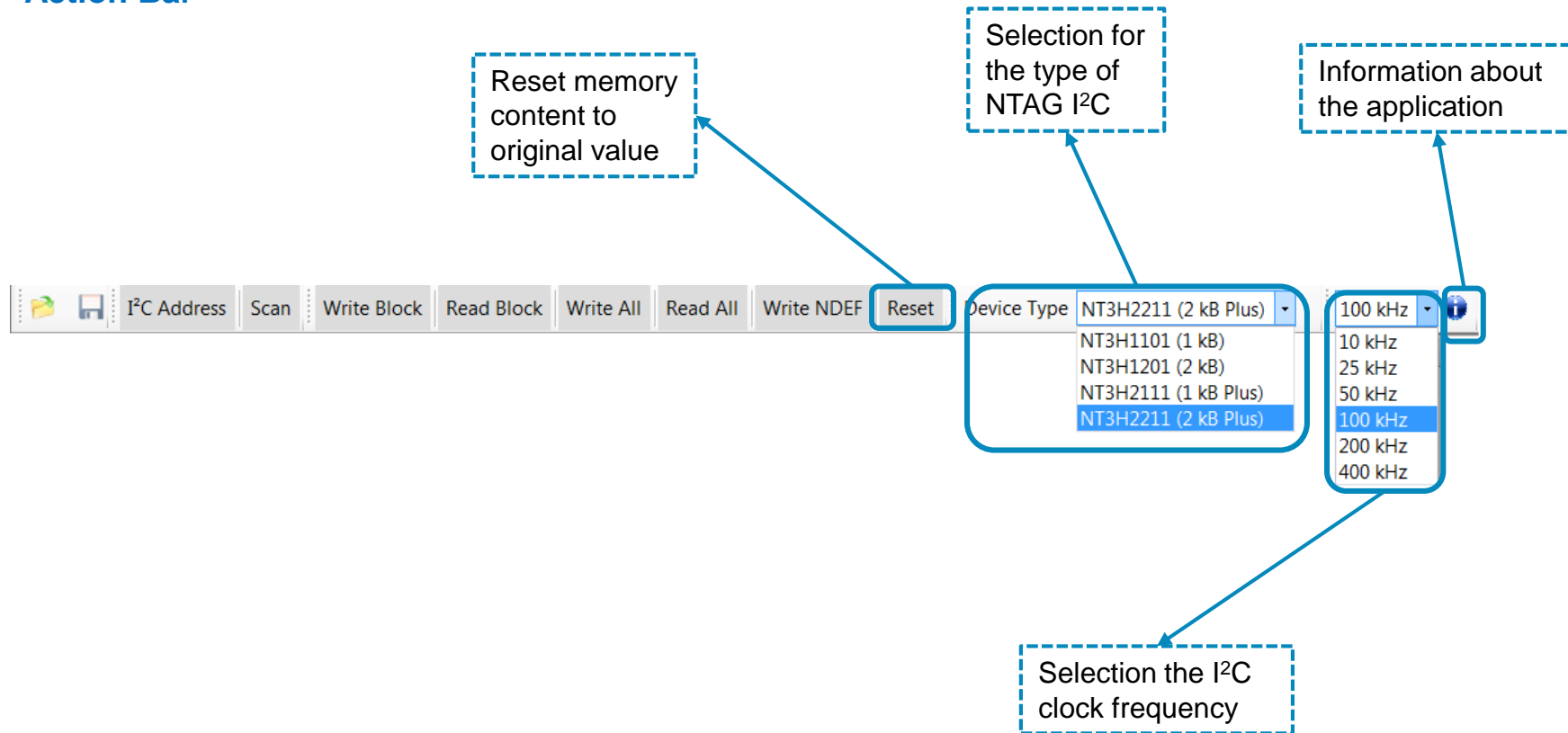
On the left side, a sidebar lists memory addresses and their functions: 0x3A0: Configuration registers, 0x400: User memory (R/W), 0xF80: SRAM (R/W), and 0xFE0: Session registers. A blue dashed box highlights the 'Write NDEF Message' button in this sidebar, with a blue arrow pointing to the 'Write NDEF' button in the toolbar.

The main area of the interface shows two hex grids. The left grid displays memory addresses from 00 to 0A and their corresponding hex values. The right grid displays the ASCII representation of the data, showing the text 'Smart Poster' followed by a URL and a AAR.

In the foreground, a 'Write NDEF message' dialog box is open. It has two tabs: 'Text NDEF message' and 'Default NDEF message'. The 'Text NDEF message' tab is active, showing a text input field and a 'Write' button. The 'Default NDEF message' tab shows a pre-filled message and a 'Write' button. A 'Cancel' button is located at the bottom of the dialog box.

NTAG I²C *plus* Peek and Poke

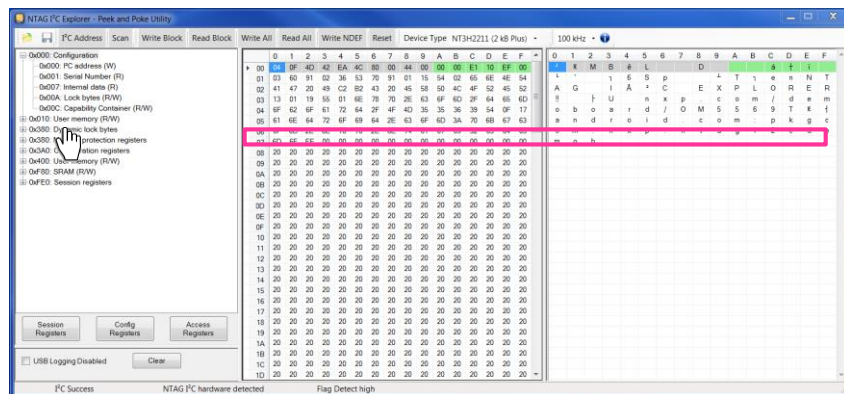
Action Bar



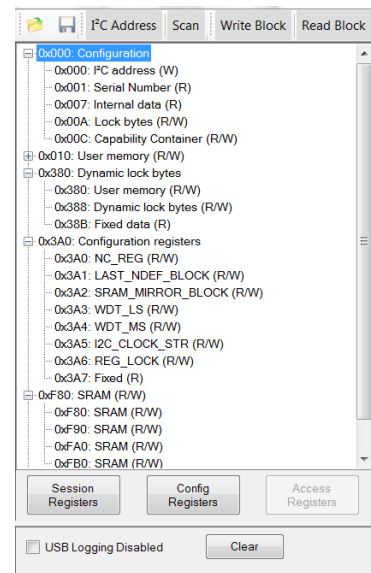
NTAG I²C *plus* Peek and Poke

Memory Block Selection

- ▶ Fluent and intuitive graphical exploration of the tag memory
- ▶ The panels are connected. What is selected in one, is highlighted in the others.



- ▶ The Tree View offers a better navigation through the different memory sections.



NTAG I²C *plus* Peek and Poke

Memory Block Selection – Unprotected Memory

The screenshot displays the NTAG I²C *plus* software interface. The top toolbar includes buttons for I²C Address, Scan, Write Block, Read Block, Write All, Read All, Write NDEF, and Reset. The Device Type is set to NT3H2211 (2 kB Plus) and the frequency is 100 kHz.

The left sidebar shows a list of memory blocks. The '0x010: User memory (R/W)' block is selected. Below the list are buttons for Session Registers, Config Registers, and Access Registers, along with a checkbox for USB Logging Disabled and a Clear button.

The main area displays a memory dump. The top table shows hexadecimal values for addresses 00 to 1D. The bottom table shows the corresponding ASCII characters.

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	04	0F	4D	42	EA	4C	80	00	44	00	00	E1	10	EF	00	
01	03	63	91	02	35	53	70	91	01	14	54	02	65	6E	4E	54
02	41	47	20	49	32	43	20	45	58	50	4C	4F	52	45	52	51
03	01	19	55	01	6E	78	70	2E	63	6F	6D	2F	64	65	6D	6F
04	62	6F	61	72	64	2F	4F	4D	35	35	36	39	54	0F	17	61
05	6E	64	72	6F	69	64	2E	63	6F	6D	3A	70	6B	67	63	6F
06	6D	2E	6E	78	70	2E	6E	74	61	67	69	32	63	64	65	6D
07	6F	5F	64	65	76	FE	00	00	00	00	00	00	00	00	00	00
08	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
09	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0A	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0B	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0C	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0D	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0E	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0F	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
10	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
11	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
12	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
13	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
14	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
15	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
16	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
17	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
18	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
19	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
1A	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
1B	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
1C	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
1D	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	J	x	M	B	e	L		D								
01	L	c		1	5	S	p									
02	A	G		I	2	C		E	X	P	L	O	R	E	R	Q
03																
04																
05																
06																
07																
08																
09																
0A																
0B																
0C																
0D																
0E																
0F																
10																
11																
12																
13																
14																
15																
16																
17																
18																
19																
1A																
1B																
1C																
1D																

NTAG I²C *plus* Peek and Poke

Memory Block Selection – Read Only Memory Area

The screenshot displays the NTAG I²C *plus* software interface. The top menu bar includes options like I²C Address, Scan, Write Block, Read Block, Write All, Read All, Write NDEF, Reset, Device Type (NT3H2211 (2 kB Plus)), and a frequency setting of 100 kHz. On the left, a tree view shows memory blocks from 0x000 to 0x170, with 0x010: User memory (R/W) selected. The main area features a large hex dump table with columns for address (00 to 1D) and data (0 to F). The data for address 01 is highlighted in blue and contains the ASCII string "LcMBrêLSpTteñNTAG". Below the hex dump, there are buttons for Session Registers, Config Registers, and Access Registers, along with a checkbox for USB Logging Disabled and a Clear button.

Address	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	04	0F	4D	42	EA	4C	80	00	44	00	00	00	E1	10	EF	00
01	03	63	91	02	35	53	70	91	01	14	54	02	65	6E	4E	54
02	41	47	20	49	32	43	20	45	58	50	4C	4F	52	45	52	51
03	01	19	55	01	6E	78	70	2E	63	6F	6D	2F	64	65	6D	6F
04	62	6F	61	72	64	2F	4F	4D	35	35	36	39	54	0F	17	61
05	6E	64	72	6F	69	64	2E	63	6F	6D	3A	70	6B	67	63	6F
06	6D	2E	6E	78	70	2E	6E	74	61	67	69	32	63	64	65	6D
07	6F	5F	64	65	76	FE	00	00	00	00	00	00	00	00	00	00
08	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
09	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0A	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0B	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0C	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0D	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0E	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
0F	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
10	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
11	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
12	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
13	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
14	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
15	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
16	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
17	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
18	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
19	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
1A	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
1B	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
1C	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20
1D	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20	20

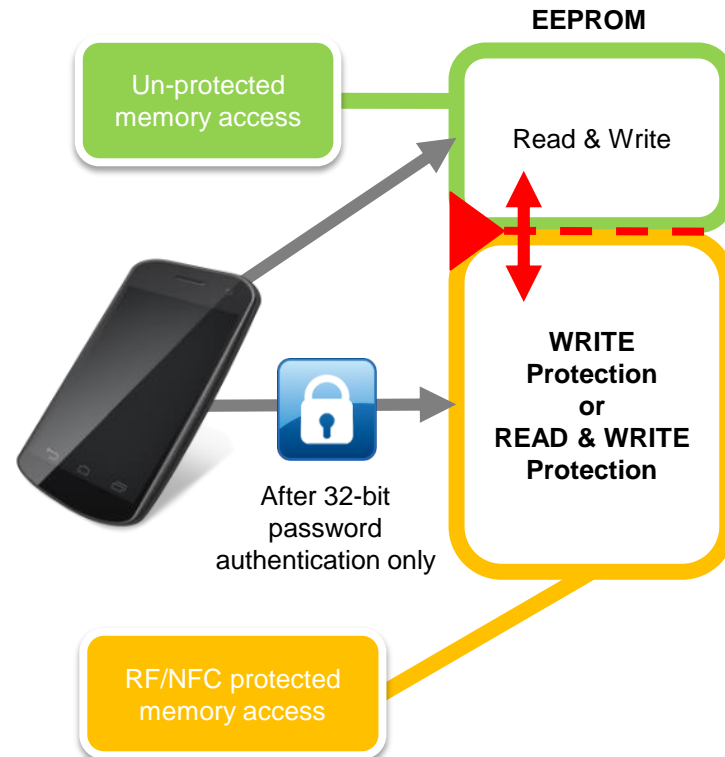
Memory access configuration

From RF/NFC interface



- ▶ 32-bit password
- ▶ 16-bit PACK (password auth. acknowledge response)
- ▶ Optionally limited number of unsuccessful authentications
 - up to 27 negative attempts
- ▶ Write or read/write memory access can be restricted to be allowed only after password authentication
- ▶ Memory can be split in open and protected segments
 - Memory boundary is configurable

NFC page address (Sector 0)		Byte number from NFC perspective			
Dec	Hex	0	1	2	3
227	E3h	RFU	RFU	RFU	AUTH0
228	E4h	ACCESS	RFU	RFU	RFU
229	E5h	PWD			
230	E6h	PACK		RFU	RFU
231	E7h	PT_I2C	RFU	RFU	RFU



NTAG I²C *plus* Peek and Poke

Access Registers

The screenshot shows the 'Access Registers' configuration window for an NT3H2211 (2) device. The window is divided into several sections: AUTH0, ACCESS, PT_I2C, and PACK. Annotations with colored dashed boxes and arrows point to specific fields and controls:

- Starting memory address of the protected area.** Points to the '0x040: User memory (R/W)' and '0x050: User memory (R/W)' entries in the top left.
- Limit of times of false password attempts** Points to the 'AUTH0' field, which contains the value '03'.
- Password protection for pass-through and mirror mode** Points to the 'SRAM_PROT' checkbox, which is checked.
- Password protection for Sector1 for NTAG I²C *plus* 2K version.** Points to the '2K_PROT' checkbox, which is unchecked.
- Type of Access to protected area from I²C perspective** Points to the 'I2C_PROT' dropdown menu, which is set to '00: Entire memori'.
- Sets if the protection is to write or to read and write** Points to the 'NFC_PROT' checkbox, which is checked.
- 32bit password to protect the memory** Points to the 'Password' field, which contains '00000000'.
- 16bit password acknowledge.** Points to the 'PACK' field, which contains '0000'.
- The fields PWD and PACK cannot be read and always returns 00.00. Be aware when writing, PWD and PACK are overwritten.** This text is located below the Password and PACK fields.

At the bottom left, a 'Report Output' section shows the following data:

```
Report Output Report ID: 0
Total Bytes: 0x14
Transaction identifier: 0x01
Session identifier: 0x29
HID I2C Request: 0x00
```

The background of the window shows a hex dump of memory data, with columns labeled A through F and rows numbered 00 through 1D.

NTAG I²C *plus* Peek and Poke

Session Registers

Sets the Pass Through mode, the event on FD pin, the SRAM mirroring and the data flow direction.

Enables I²C clock stretching.

I²C block address containing last of NDEF message

Watchdog time control

Lock of memory Access from I²C or RF, if NDEF is read, if SRAM is ready to be read by I²C or by RF, error during EEPROM operation and if RF field is present.

The screenshot shows the 'Session Registers' window with the following fields and controls:

- NC_REG : 0xFE:0**
 - ☐ I2C_RST_ON_OFF
 - ☐ PTHRU_ON_OFF
 - FD_OFF: 00: Field switched off
 - FD_ON: 00: Field presence
 - ☐ SRAM_MIRROR_ON_OFF
 - ☒ TRANSFER_DIR
 - Buttons: Read NC_REG, Write NC_REG
- I2C_CLOCK_STR : 0xFE:5**
 - ☒ I2C_CLOCK_STR: Enabled
 - Button: Read I2C_STR
- LAST_NDEF_BLOCK : 0xFE:1**
 - Last BLOCK NDEF message: 00
 - Buttons: Read NDEF, Write NDEF
- SRAM_MIRROR_BLOCK : 0xFE:2**
 - I²C block address: F8
 - Buttons: Read SM_REG, Write SM_REG
- WDT : 0xFE:[4:3]**
 - Watchdog time-out: 20.000 ms
 - Buttons: Read WDT, Write WDT
- NS_REG : 0xFE:6**
 - ☐ NDEF_DATA_READ (RO)
 - ☐ I2C_LOCKED
 - ☐ RF_LOCKED (RO)
 - ☐ SRAM_I2C_READY (RO)
 - ☐ SRAM_RF_READY (RO)
 - ☐ EEPROM_WR_ERR
 - ☐ EEPROM_WR_BUSY (RO)
 - ☐ RF_FIELD_PRESENT (RO)
 - Buttons: Read NS_REG, Write NS_REG

Buttons at the bottom: Read All

I²C block address of SRAM when mirrored into the User memory.

NTAG I²C *plus* Peek and Poke

Configuration Registers

All registers are the same as in the session registers

The screenshot shows a hex editor with a grid of memory addresses and values. Overlaid on this is a 'Configuration Registers' dialog box. The dialog box contains several sections for configuring different registers:

- NC_REG : 0x3A:0**
 - ☐ I2C_RST_ON_OFF
 - ☐ PTHRU_ON_OFF
 - FD_OFF: 00: Field switched off
 - FD_ON: 00: Field presence
 - ☐ SRAM_MIRROR_ON_OFF
 - ☒ TRANSFER_DIR
- LAST_NDEF_BLOCK : 0x3A:1**
 - Last BLOCK NDEF message: 00
- WDT : 0x3A:[4:3]**
 - Watchdog time-out 20.000 ms
- SRAM_MIRROR_BLOCK : 0x3A:2**
 - PC block address: F8
- REG_LOCK : 0x3A:6**
 - ☐ I2C_LOCKED
 - ☐ RF_LOCKED
- I2C_CLOCK_STR : 0x3A:5**
 - ☒ I2C_CLOCK_STR: Enabled

At the bottom of the dialog box are three buttons: 'Write Config', 'Read Config', and 'Close'.

NTAG I²C *plus*

Developing applications

How to develop applications around NTAG I²C *plus*

Available material
to develop your
own solutions

Firmware

Peek and Poke

Pc Windows Application

Android Application

How to develop applications around NTAG I²C *plus*

- ▶ Develop and test your own applications.
- ▶ The Peek and Poke, Windows app and Android application are a reusable code.
- ▶ Versatility of APIs to develop around NTAG I²C *plus* (in Java, C# and C++).
- ▶ Environments: Windows and Android platform.

```
53     return (int)busSpeed;
54 }
55
56
57
58 private byte[] CreateCommandToInitI2CPort()
59 {
60     byte[] data = new byte[16];
61     data[0] = 0x0C; // total number of bytes
62     data[1] = 0x00; // Transaction identifier
63     data[2] = 0x29; // Session identifier
64     data[3] = 0x01; // HID_I2C_REQ_INIT_PORT
65     data[4] = (byte)(this.busSpeed & 0xFF); // I2C bus speed
66     data[5] = (byte)((this.busSpeed >> 8) & 0xFF);
67     data[6] = (byte)((this.busSpeed >> 16) & 0xFF);
68     data[7] = (byte)((this.busSpeed >> 24) & 0xFF);
69     data[8] = 0x00;
70     data[9] = 0x00;
71     data[10] = 0x00;
72     data[11] = 0x00;
73     data[12] = 0x00;
74     data[13] = 0x00;
75     data[14] = 0x00;
76     data[15] = 0x00;
77     return data;
78 }
79
80 /** @brief Initialize the communication with the port
81  *
82  * @param device is the object representing the device to connect with.
83  * @return the response from the command to init the port.
84  */
85 public I2CData init(I2C_Device device)
86 {
87     var command = CreateCommandToInitI2CPort();
88     var returnVal = device.performTransaction(command);
89     initialised = true;
90     return returnVal;
91 }
92
93 /** @brief Reinitialize the communication with the port
94  *
95  * @param device is the object representing the device to connect with.
96  * @param busSpeedInKHz is the bus speed on the bus for the communication
97  * @return the response from the command to init the port.
98  */
99 public I2CData reinit(int busSpeedInKHz, I2C_Device device)
100 {
101     I2CData result = null;
102     setBusSpeedInKHz(busSpeedInKHz * 1000);
103     if (device.isConnected())
104     {
105         result = init(device);
106     }
107     return result;
108 }
109 }
110 }
```

How to develop applications around NTAG I²C *plus*

Available material
to develop your
own solutions

Firmware

Peek and Poke

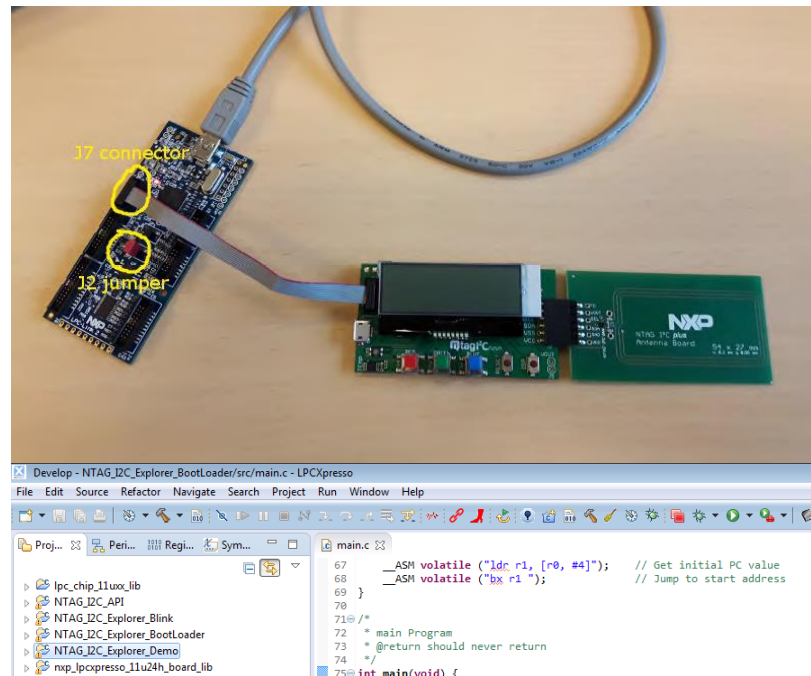
Pc Windows Application

Android Application

How to develop applications around NTAG I²C *plus*

Firmware development

- ▶ Firmware consists of:
 - The bootloader
 - The Explorer Demo Application
 - The Blink
- ▶ LPCXpresso software
<https://www.lpcware.com/lpcxpresso/downloads/windows>
- ▶ Use LPCLink2 to connect (or flash)
- ▶ An application can also be flashed with Android application.



How to develop applications around NTAG I²C *plus*

Available material
to develop your
own solutions

Firmware

Peek and Poke

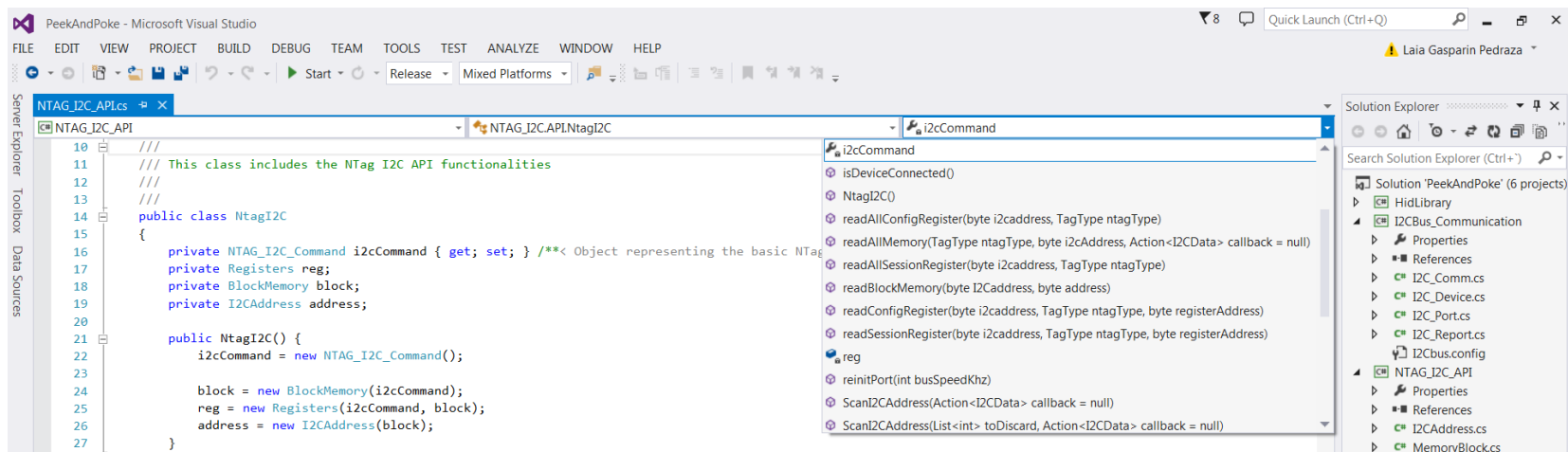
Pc Windows Application

Android Application

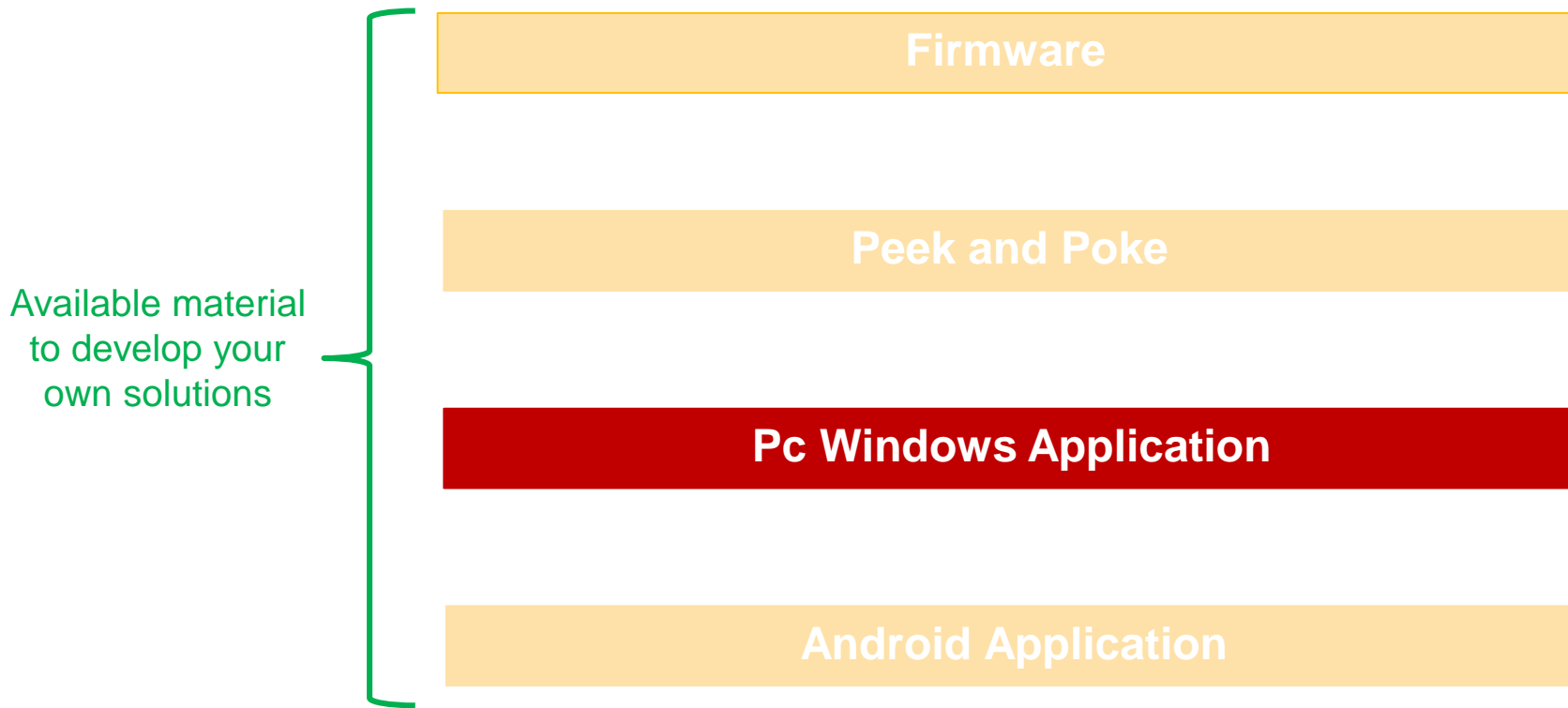
How to develop applications around NTAG I²C *plus*

Peek and Poke API

- ▶ API directly offers the functionalities of the Peek and Poke (Read all memory, read config registers, ...)
- ▶ The architecture of the Peek and Poke offers several layers of abstraction
 - NTAG I²C Communication
 - NTAG I²C Commands
 - NTAG I²C API
- ▶ Developed in C#

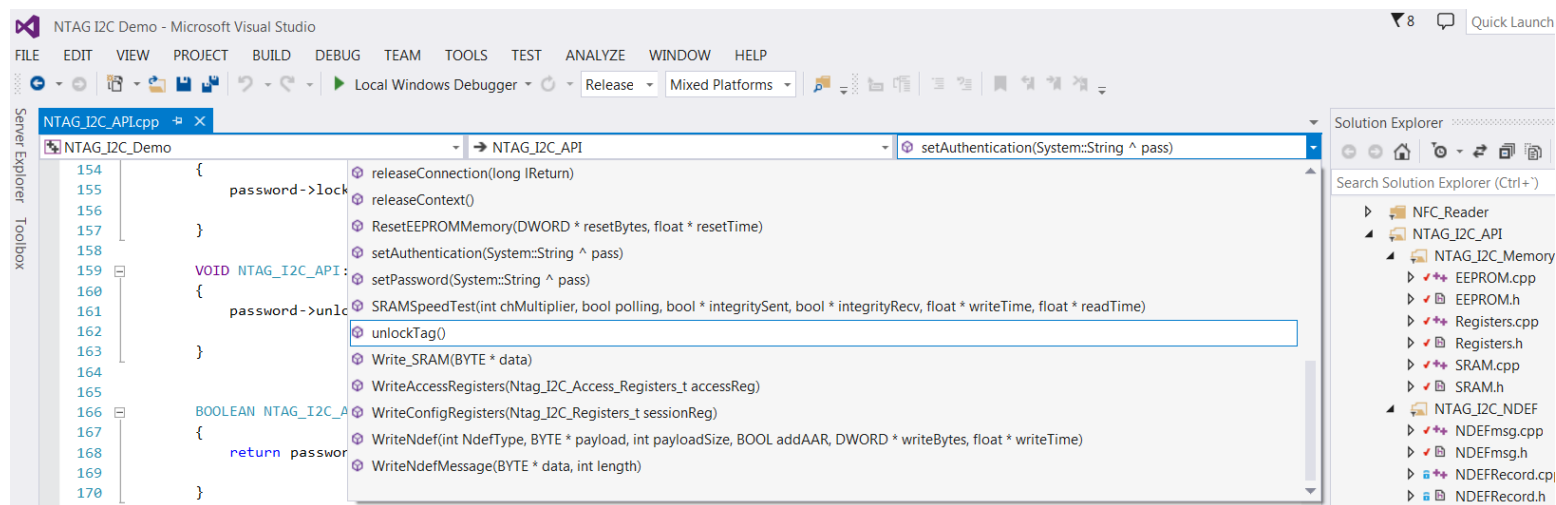


How to develop applications around NTAG I²C *plus*

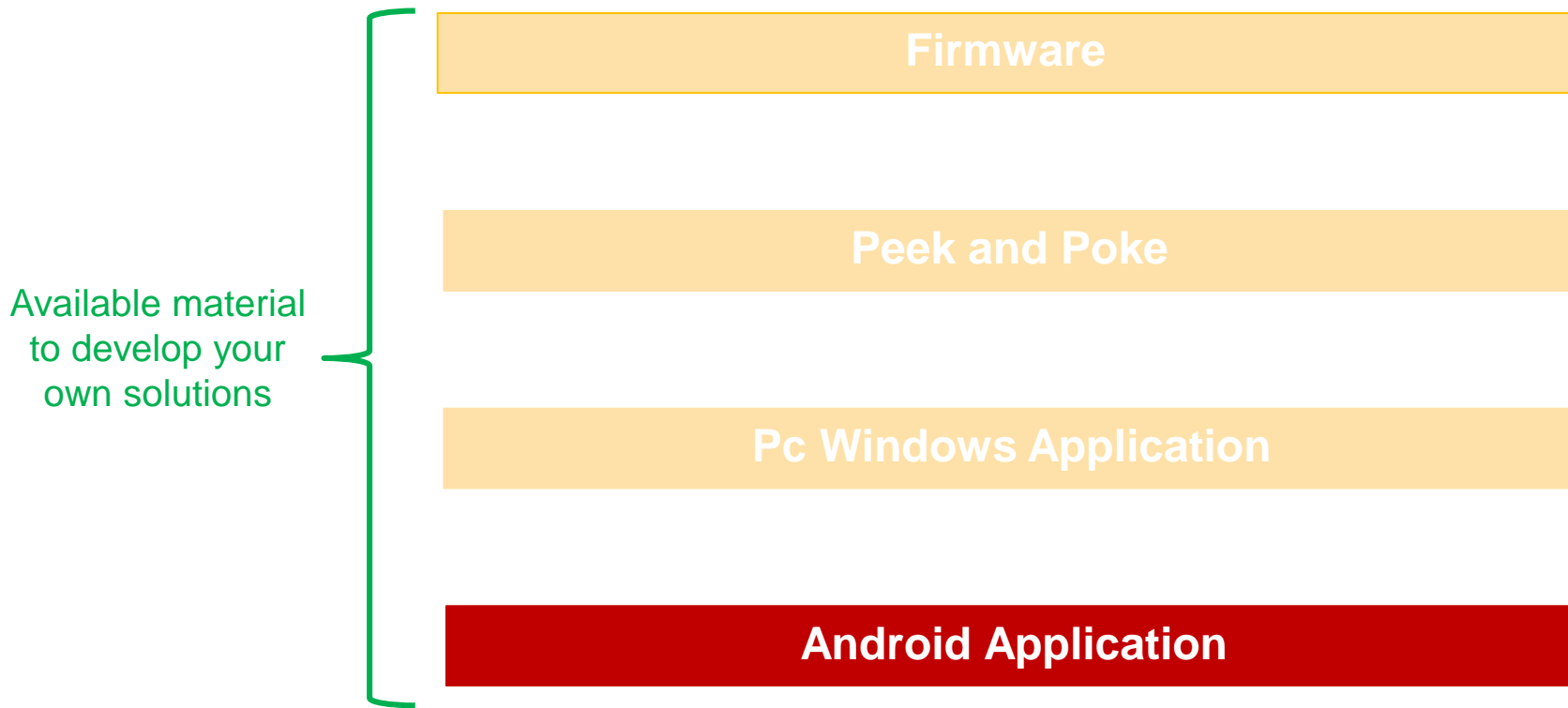


How to develop applications around NTAG I²C *plus* Windows App API

- ▶ Microsoft Visual Studio.
- ▶ Developed in C++
- ▶ API directly offers the functionalities of the Windows app (write NDEF, read EEPROM, set Password,...)
- ▶ PCSC communication.
- ▶ Easy to develop your own application using this code as example and the available API.

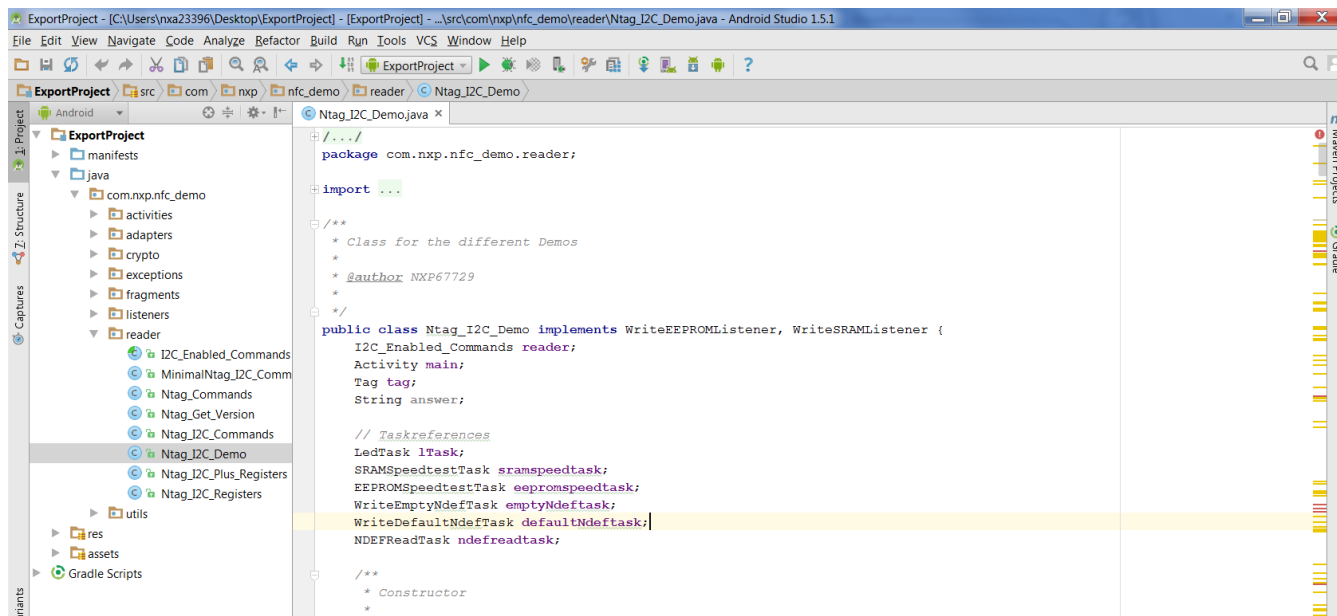


How to develop applications around NTAG I²C *plus*



How to develop applications around NTAG I²C *plus* Android app

- ▶ Source code for Android Studio to develop your own app.
- ▶ Faster development to go to market.
- ▶ Developed in Java.
- ▶ APIs available for the RF commands and the higher level functionalities (read SRAM block, ...)



Wrap up

NTAG I²C *plus* is supported by advanced tools



NFC frontend development kit OM5569-NT322E
Available at eDemoboard and Distis



Windows and Android application
*A mobile and desktop application to test features of the NTAG I²C *plus**



Peek and Poke
A desktop application to navigate and explore the memory.



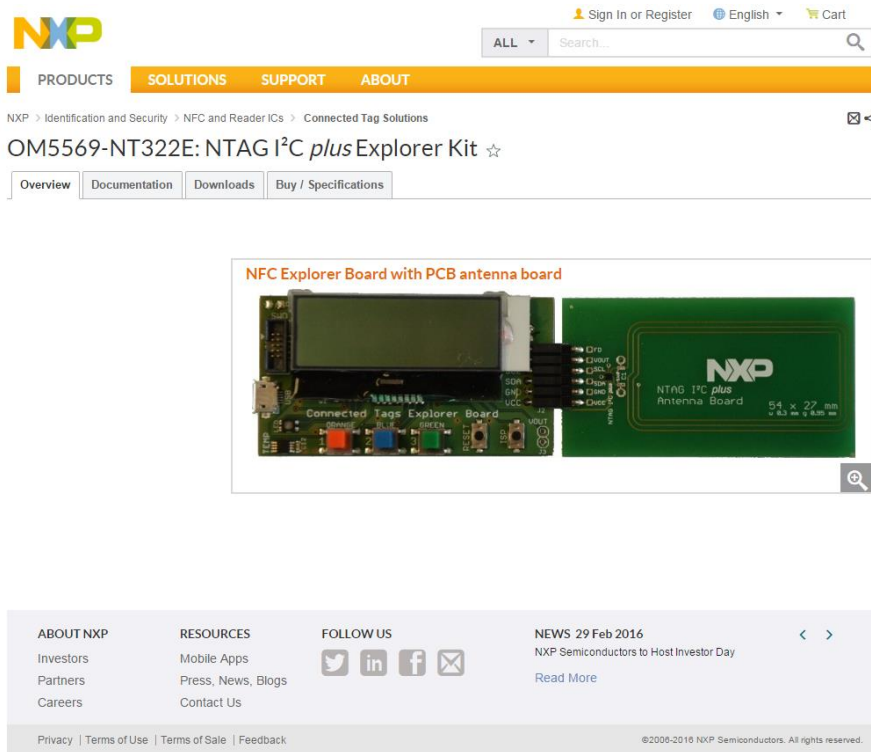
Android code, C# and C++ APIs
Example code and APIs to develop application upon it.



Do you need more?

Resources and useful links

- ▶ NFC Everywhere
<http://www.nxp.com/nfc>
- ▶ NT3H2111/2211: NTAG I²C *plus* product website
http://www.nxp.com/products/identification-and-security/nfc-and-reader-ics/connected-tag-solutions/ntag-ic-plus-nfc-forum-type-2-tag-compliant-ic-with-ic-interface:NT3H2111_2211
- ▶ OM5569-NT322E demokit website
<http://www.nxp.com/products/identification-and-security/nfc-and-reader-ics/connected-tag-solutions/ntag-ic-plus-i-explorer-kit:OM5569-NT322E>
- ▶ NXP Tech community
<http://nxpcommunity.force.com/community/CommunityOverview>



The screenshot displays the NXP website's product page for the OM5569-NT322E: NTAG I²C *plus* Explorer Kit. The page features a navigation bar with links to PRODUCTS, SOLUTIONS, SUPPORT, and ABOUT. Below the navigation bar, the product name is prominently displayed, followed by a star icon. A tabbed interface shows the 'Overview' tab selected, with other tabs for 'Documentation', 'Downloads', and 'Buy / Specifications'. A large image of the 'NFC Explorer Board with PCB antenna board' is shown, featuring a green PCB with a black antenna board attached. The board is labeled 'Connected Tags Explorer Board' and 'NTAG I²C plus Antenna Board'. The bottom of the page includes a footer with sections for 'ABOUT NXP' (Investors, Partners, Careers), 'RESOURCES' (Mobile Apps, Press, News, Blogs, Contact Us), 'FOLLOW US' (Twitter, LinkedIn, Facebook, Email), and 'NEWS 29 Feb 2016' (NXP Semiconductors to Host Investor Day). The footer also contains a privacy policy link and a copyright notice: '©2006-2016 NXP Semiconductors. All rights reserved.'

Thank you