

# CLRC663 *plus*

BEST PERFORMANCE AT LOWEST POWER CONSUMPTION

JORDI JOFRE  
NFC READERS  
NFC EVERYWHERE  
21/06/2017



PUBLIC



SECURE CONNECTIONS  
FOR A SMARTER WORLD

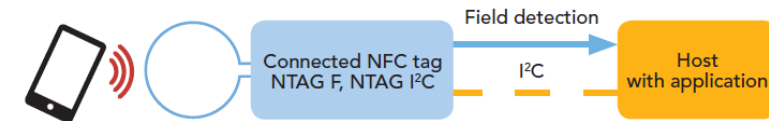
# CLRC663 *plus* product positioning



# NFC product portfolio

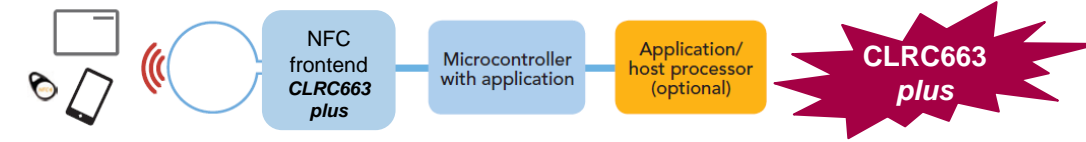
## Connected NFC tag solutions

Our connected NFC tag solutions include a NFC Forum RF interface, an EEPROM, and a field-detection function (NTAG F) or a field-detection function with an I<sup>2</sup>C interface (NTAG I<sup>2</sup>C *plus*).



## NFC frontend solutions

Our stand-alone frontends, which work seamlessly with the NFC Reader Library, are the most flexible way to add NFC to a system.

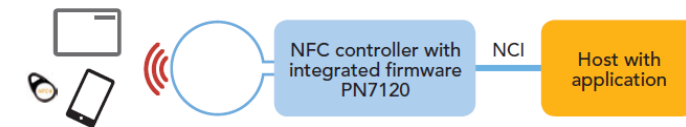


## NFC controller solutions

Our NFC controller solutions enable higher integration with fewer components combining an NFC frontend with an advanced 32-bit microcontroller.

Options include integrated firmware, for an easy, standardized interface, or a freely programmable microcontroller with the ability to load fully-custom applications.

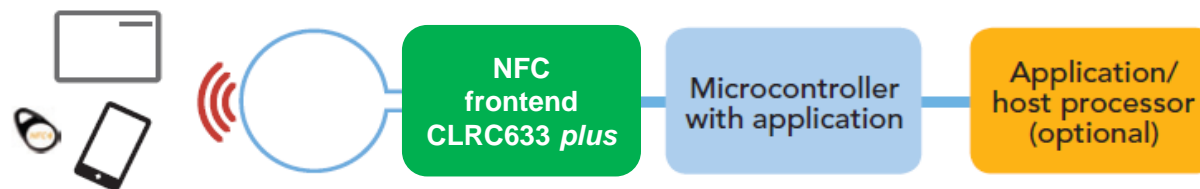
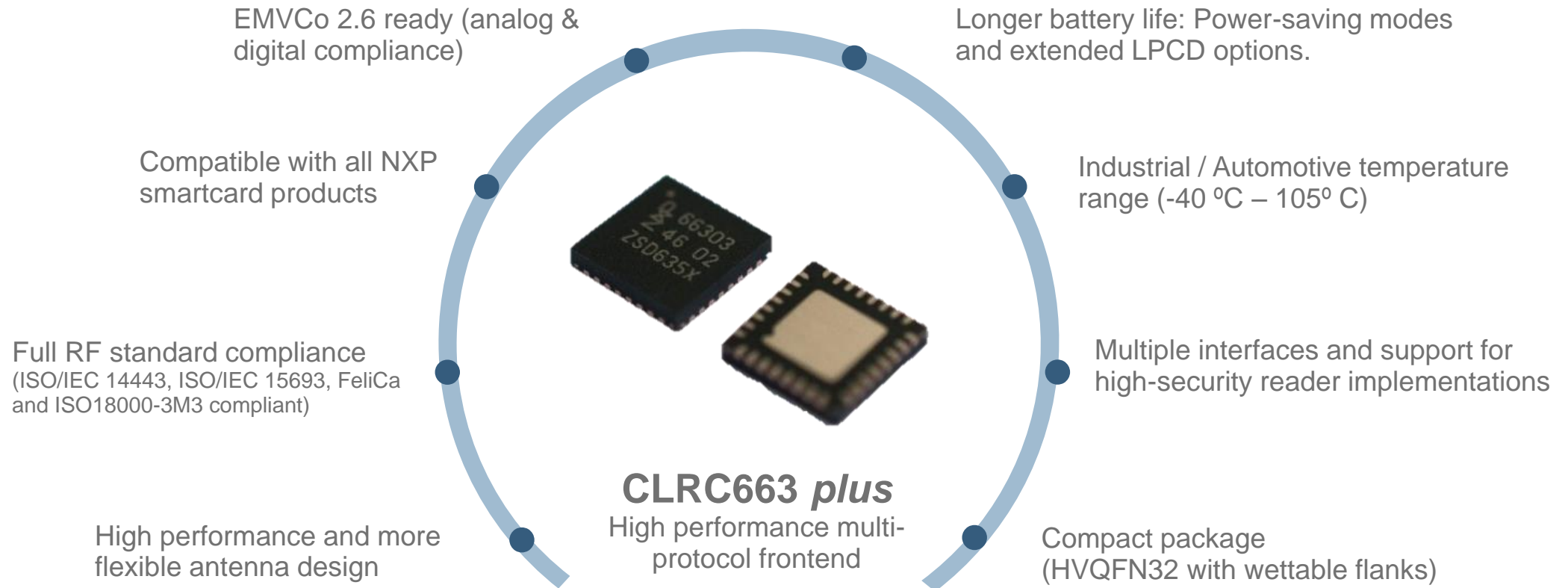
### Integrated Firmware



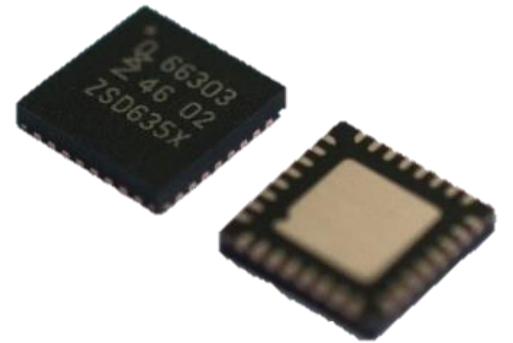
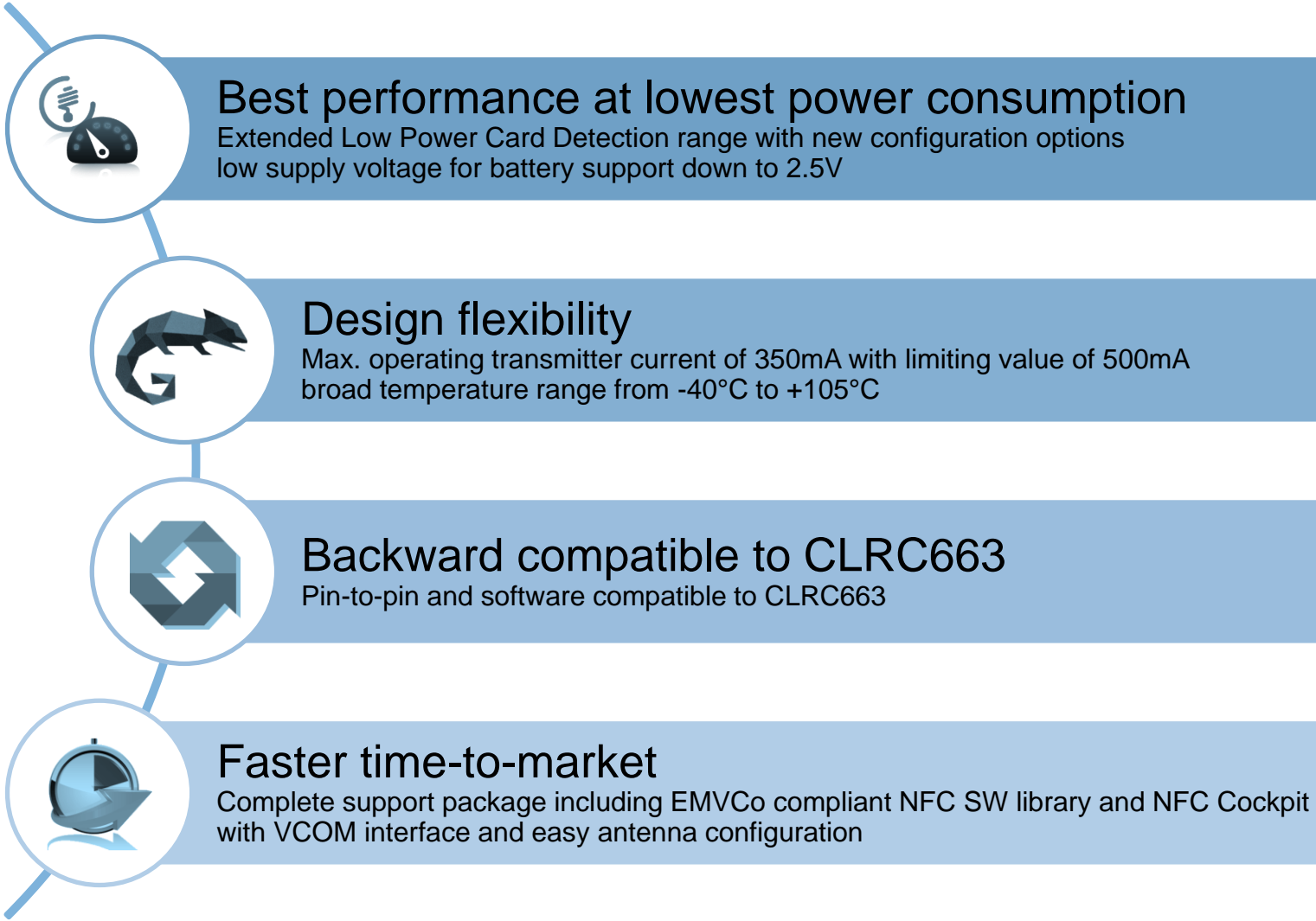
### Customizable Firmware



# CLRC663 *plus* – Push your design further



# CLRC663 *plus* key benefits

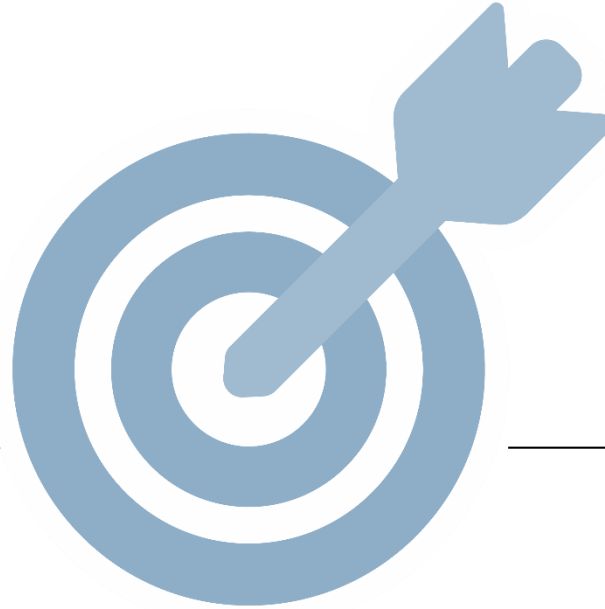


# CLRC663 *plus* target markets



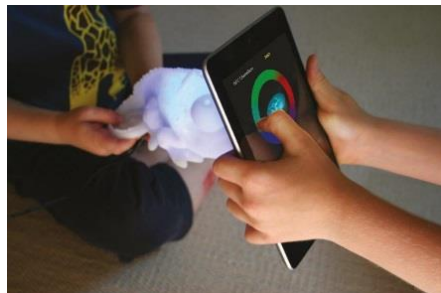
## ACCESS CONTROL & INDUSTRIAL

- Broad temperature range
- Pin-to-pin and SW compatible to CLRC663



## PAYMENT TERMINALS

- Highest transmitter current
- EMVCo 2.6 L1 analog and digital compliant



## GAMING

- Extended Low Power Card Detection range with new configuration options
- Low supply voltage for battery support down to 2.5 V

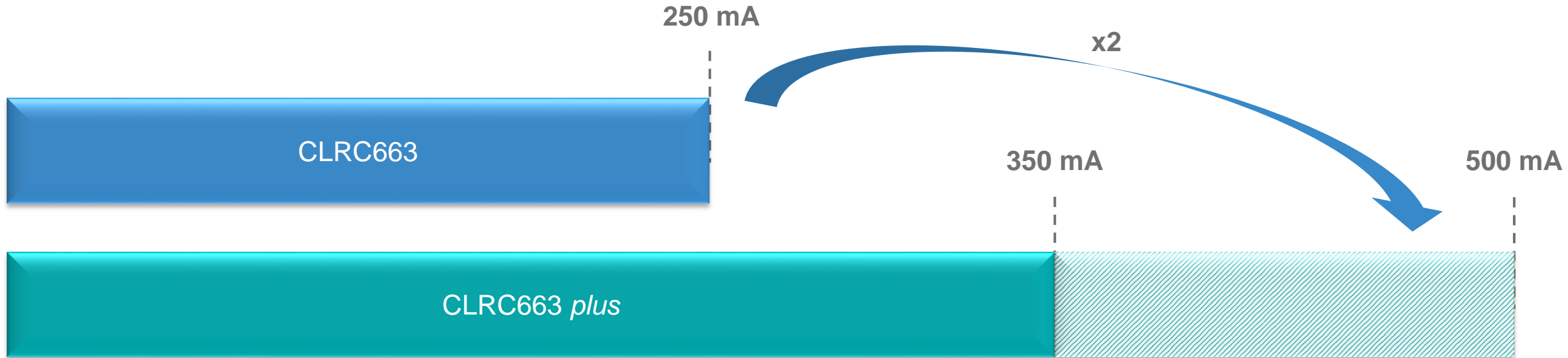
# CLRC663 *plus* vs PN5180 and PN7462

Feature	CLRC663 <i>plus</i>	PN5180	PN7462	Comment
Package	HVQFN32	HVQFN40 TFBGA64	HVQFN64	CLRC663 <i>plus</i> is pin-to-pin compatible with CLRC663
RF transmitter supply voltage	2.5 to 5.5V	2.7 to 5.5V	3 to 5.5V	CLRC663 <i>plus</i> enables better support for battery powered systems
General Purpose Input/Output pins (e.g. to drive LEDs)	4 up-to 8	up-to 7 outputs only	12 up-to 21	PN5180 has up-to 7 general purpose outputs on TFBGA64 package only
Max. operating transmitter current	350mA (lim. 500mA)	250mA with DPC	250mA with DPC	CLRC663 <i>plus</i> enables more flexibility in the antenna design
Temperature range	-40 to +105°C	-30 to +85°C	-40 to +85°C	CLRC663 <i>plus</i> has an automotive or industrial temperature range
Low power card detection	range: very good power: best	range: best power: good	range: best power: good	CLRC663 <i>plus</i> offers the lowest power consumption
Complete set of field proven software libraries	NFC & EMVCo	Full NFC & EMVCo	Full NFC & EMVCo	Full NFC forum certified library; EMVCo 2.6
Waveform Control	Yes	Yes (adaptive)	Yes (adaptive)	Adaptive Waveform Control improves wave shape stability under detuned conditions
Adaptive Range Control	No	Yes	Yes	Adaptive Range Control increases sensibility and robustness under detuned conditions
Freely programmable MCU (flash)	No	No	Cortex M0 (160kB)	PN7462 enables an 1-chip reader solution
Host interfaces	SPI, I <sup>2</sup> C, UART	SPI	USB, HSUART, SPI, I <sup>2</sup> C	PN7462 has also two master interfaces (SPI, I <sup>2</sup> C) and one contact reader interface
SAM Interface	Yes with X-mode	No	Yes	The SAM interface allows to store keys in a secure container

# CLRC663 *plus* compared to CLRC663



# Higher operating transmitter current



Maximum operating transmitter current increases by 40% for CLRC663 *plus* with 2x the limiting value of the CLRC663

# Larger operating temperature range



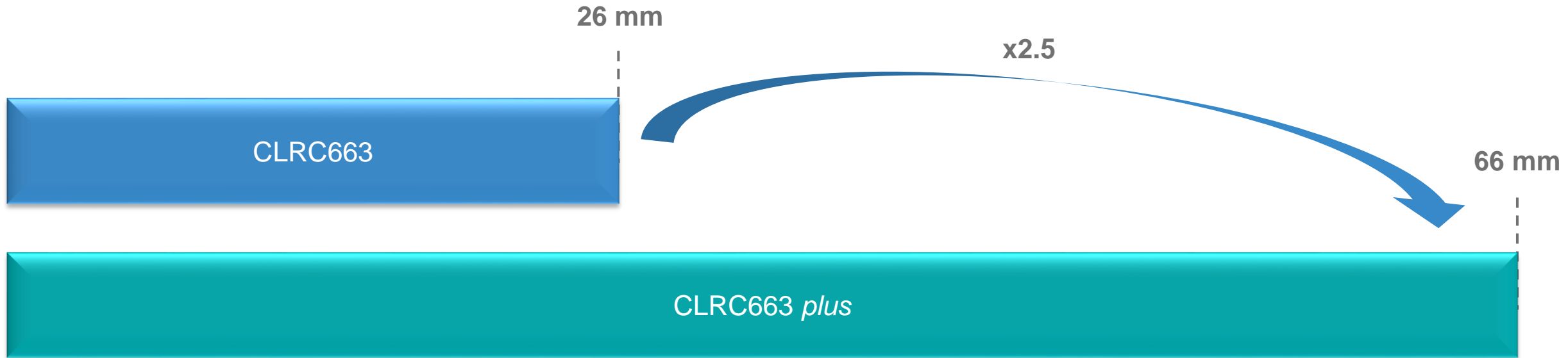
CLRC663 *plus* has an automotive or industrial operating temperature range: -40 to +105°C

# Lower supply voltage for battery-based systems



CLRC663 *plus* enables better support for  
battery powered systems

# New LPCD configuration options enabling up to 2.5x detection range\*



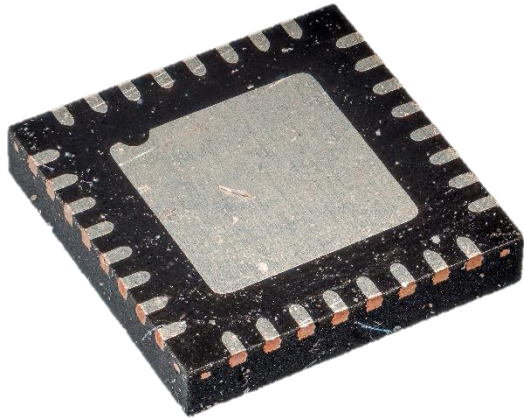
**Charge Pump:** increases the RF field strength during the RF-on time.

**LPCD Filter:** reduces the risk of fail detections, especially in case of spike noise.

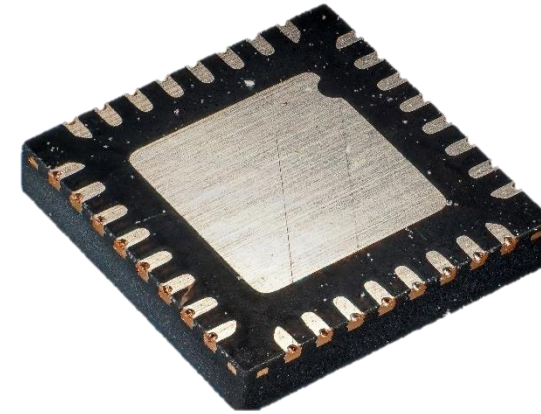
\* New LPCD configuration options are Charge Pump (enabled/disabled) and LPCD Filter (enabled/disabled).

\*\* Results obtained using a EMVCo Ref PICC with standard CLRC663 vs CLRC663 *plus* with Charge Pump and LPCD\_Filter enabled.

# New wettable flank IC package



CLRC663



CLRC663 *plus*

The CLRC663 *plus*, with wettable flank HVQFN package, enables 100% automatic visual inspection post-assembly ensuring higher quality of assembly

# Technical details

# CLRC663 *plus* – High performance multi-protocol reader

## Characteristics

- › 350mA maximum operating transmitter current with limiting value of 500mA
- › Power supply voltage: 2.5 to 5.5V
- › Extended operating temperature range: -40 to +105°C
- › 512byte FIFO buffer for highest transaction performance
- › Flexible and efficient power saving modes including hard power down, standby and low-power card detection
- › Integrated PLL provides external system clock from 27.12MHz RF crystal

## Licenses and supported standards

- › Includes NXP ISO/IEC14443-A, NXP MIFARE® and Innovatron ISO/IEC14443-B licenses
- › Crypto 1 intellectual property licensing rights
- › Hardware supports for MIFARE Classic encryption
- › EMVCo 2.6 analog compliancy on RF level and digital compliancy with NXP NFC reader library

## Interfaces

- › Host interfaces: SPI (10Mbit/s), I<sup>2</sup>C (1000kbit/s) and UART (1228.8kbit/s)
- › SAM interface in X-mode
- › Up-to 8 general purpose inputs/outputs

## Supported RF protocols

### Reader and Writer mode

- › ISO/IEC 14443A/MIFARE
- › ISO/IEC 14443B
- › JIS X 6319-4 (comparable with FeliCa1 scheme)
- › ISO/IEC 15693 (ICODE-SLI)
- › ICODE EPC UID/ EPC OTP
- › ISO/IEC 18000-3 mode 3/ EPC Class-1 HF (ICODE-ILT)

### Peer to Peer mode

- › Passive-Initiator according to ISO/IEC 14443A (106kbit/s) and FeliCa (212 and 424kbit/s)

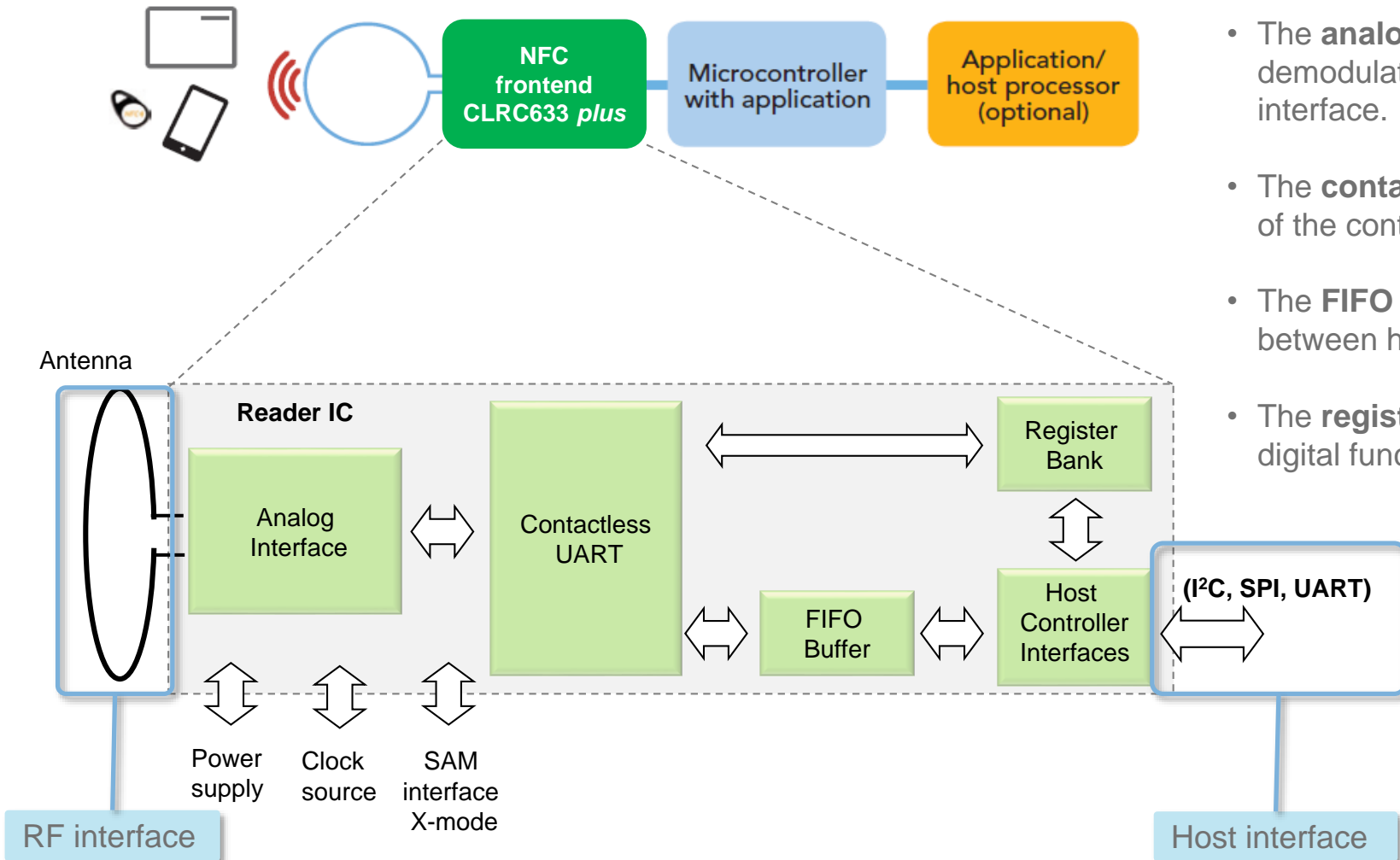
### Allows to read and write

- › All MIFARE® family: Ultralight, Classic 1K & 4K, DESFire EV1 & EV2 and Plus EV1
- › All NTAG® family incl. NTAG I<sup>2</sup>C *plus*
- › All SmartMX® family incl. SmartMX2 P40 & P60

## Packages

- › HVQFN32
- › Wettable flanks

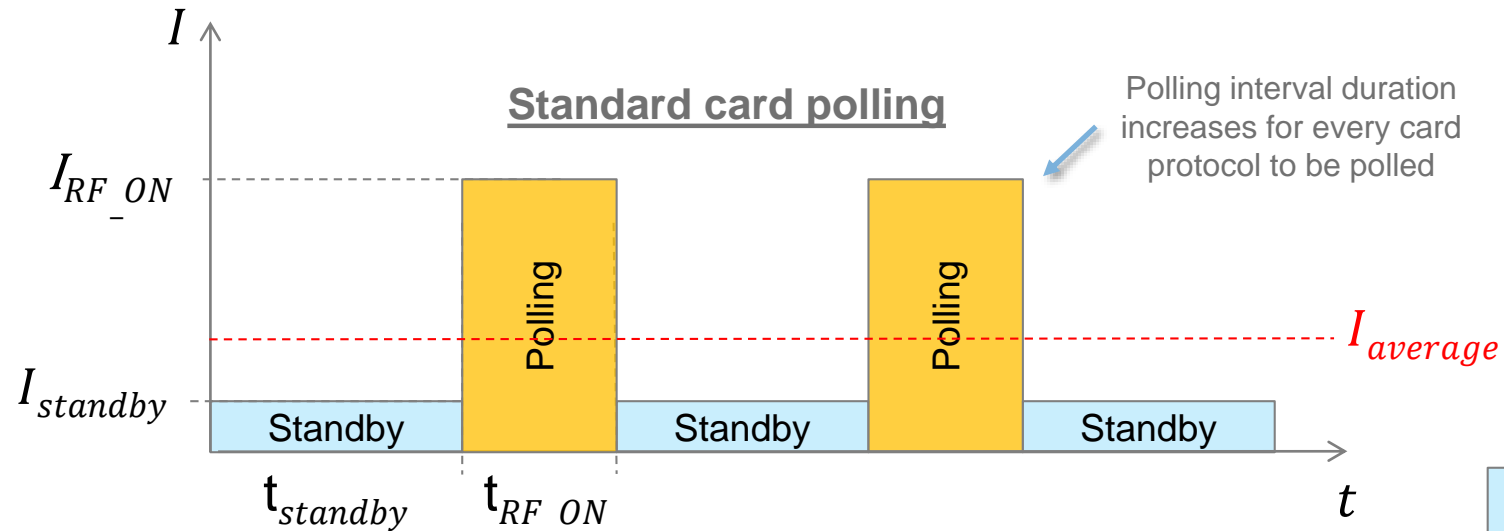
# CLRC663 *plus* simplified block diagram



- The **analog interface** handles the modulation and demodulation of the antenna signals for the contactless interface.
- The **contactless UART** manages the protocol dependency of the contactless interface settings managed by the host
- The **FIFO buffer** ensures fast and convenient data transfer between host and the contactless UART
- The **register bank** contains the settings for the analog and digital functionality

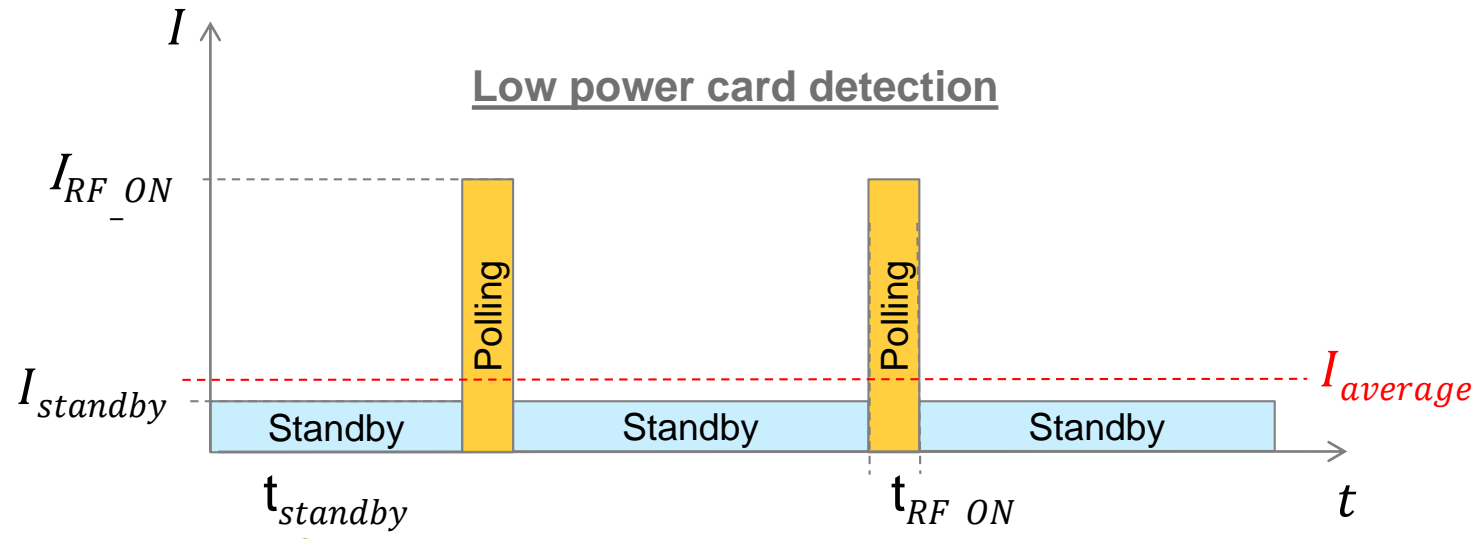


# Low Power Card Detection concept



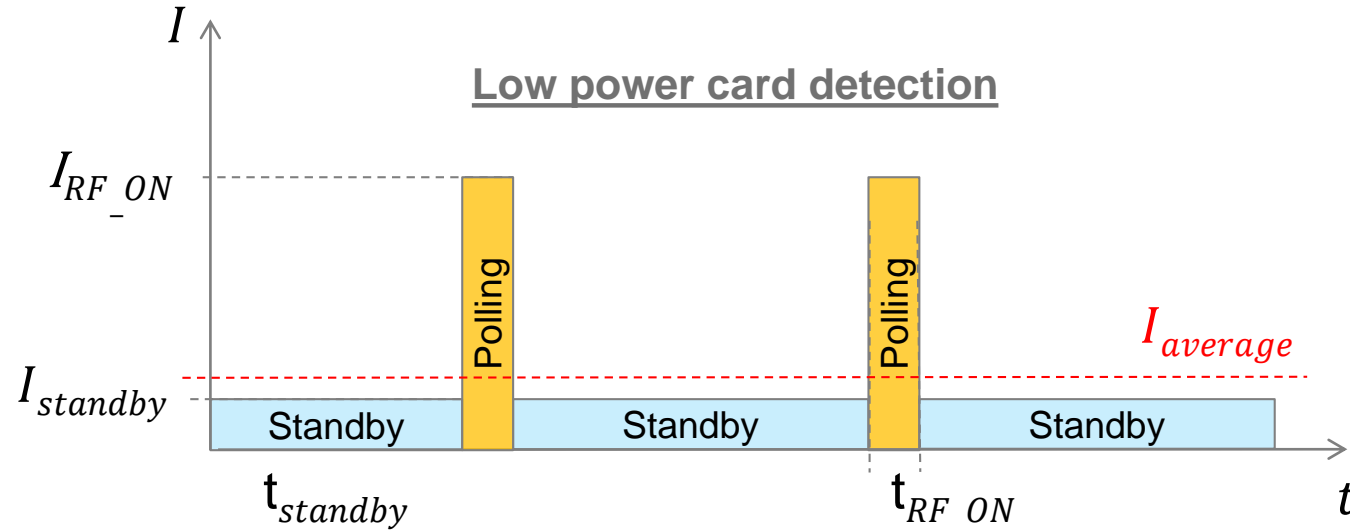
The contactless readers periodically activates the RF field to poll for the cards

$$I_{average} = \frac{I_{standby} \cdot t_{standby} + I_{RF\_ON} \cdot t_{RF\_ON}}{t_{standby} + t_{RF\_ON}}$$

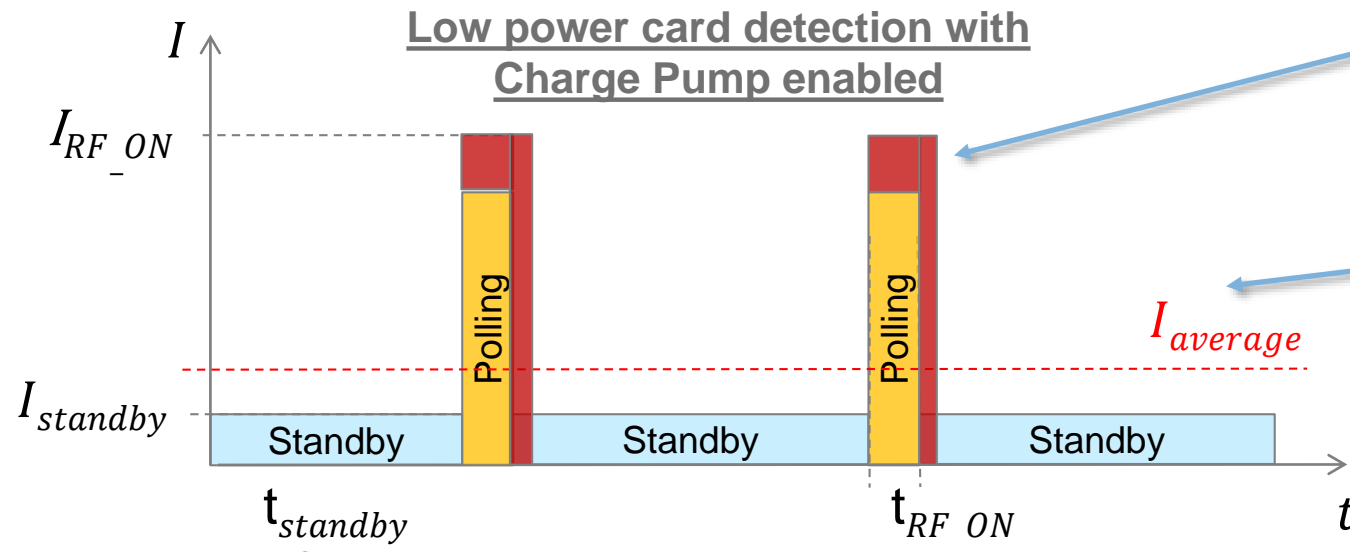


The LPCD reduces the average current consumption by providing a much shorter RF\_ON interval for the card detection

# Low Power Card Detection – Charge Pump option



Ideal for applications where the detection range might be more important

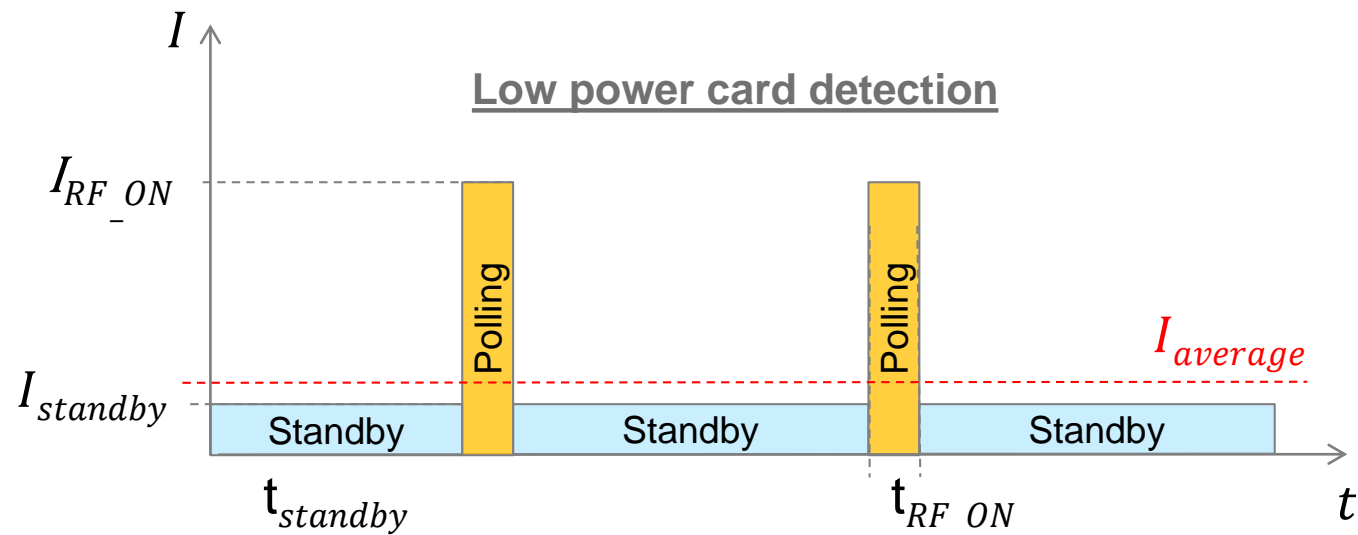


The charge pump increases the output power at TX pins (i.e RF field strength) during the RF on time.

Up to 2.5 higher detection range

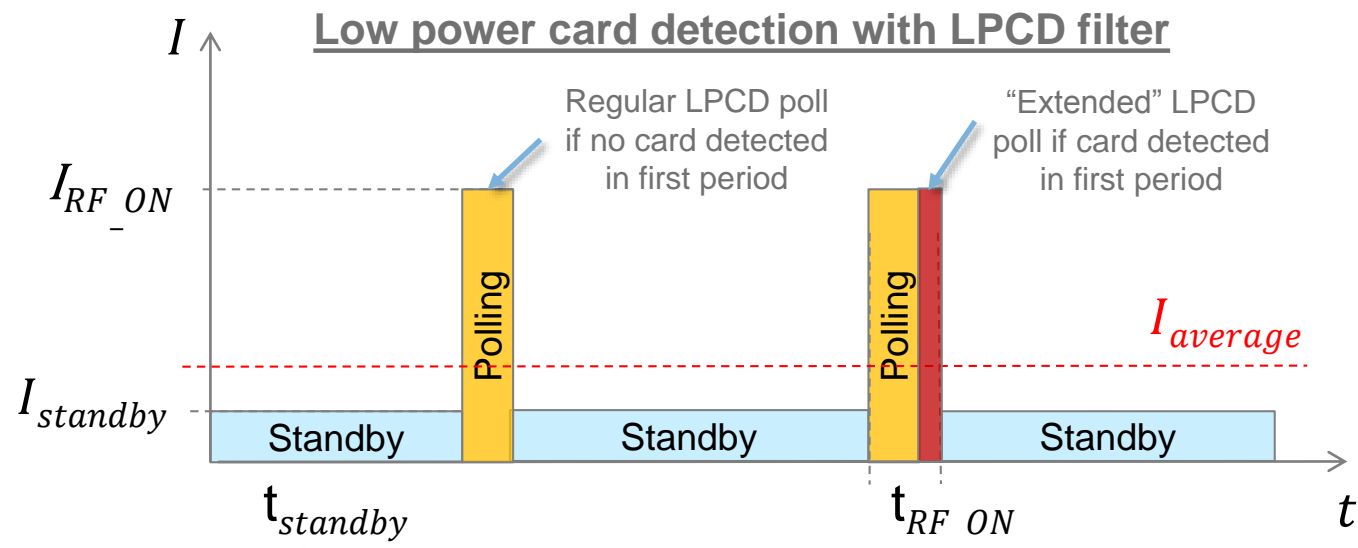
Increase current consumption

# Low Power Card Detection – LPCD filter



First period	Second period	Third period	Duration	Result
No wake up	-	-	Rfon	Return to LPCD
Wake up detected	No wake up	-	Rfon + 32 tc	Return to LPCD
Wake up detected	Wake up detected	No wake up	Rfon + 64 tc	Return to LPCD
Wake up detected	Wake up detected	Wake up detected	Rfon + 64 tc	Wake up

$t_c = 1/13.56\text{MHz} \rightarrow 32 t_c \approx 2.5\mu\text{s}$



The LPCD filter improves the card detection robustness:

- Reduces the risk of fail detections, specially the case of spike noise
- Increases average current consumption

# Product support package



# CLRC663 *plus* product support package content



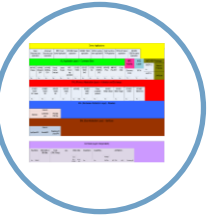
## CLRC663 *plus* NFC frontend development kit (OM26630FDK)

Development kit with integrated NXP LPC1769 MCU



## NFC cockpit v3.10

Supports PN5180, PN7462 and CLRC663 *plus*



## NFC Reader Library

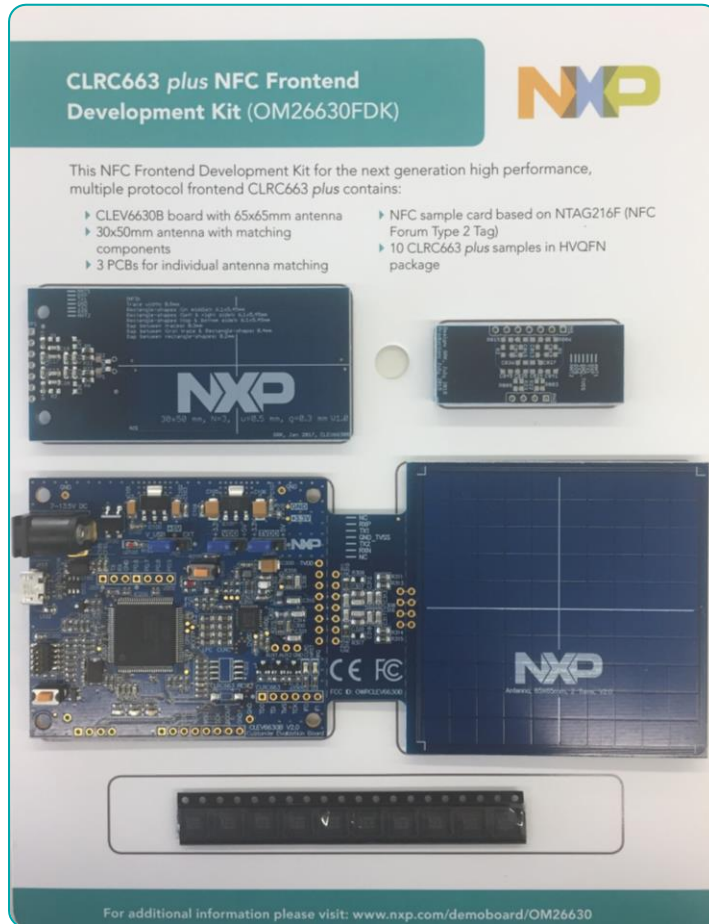
Feature complete software support library for NFC Frontend ICs



## Documentation

Datasheets and application notes for an easy ramp-up.

# CLRC663 *plus* NFC frontend development kit (OM26630FDK)



## OM26630FDK contents

- Development kit with integrated NXP LPC1769 MCU
- Straightforward antenna design with NFC Cockpit tool
- Different antenna PCBs for easy antenna matching
- Easy application development with NFC Reader Library
- CE / FCC certified CLEV6630B board

## OM26630FDK features

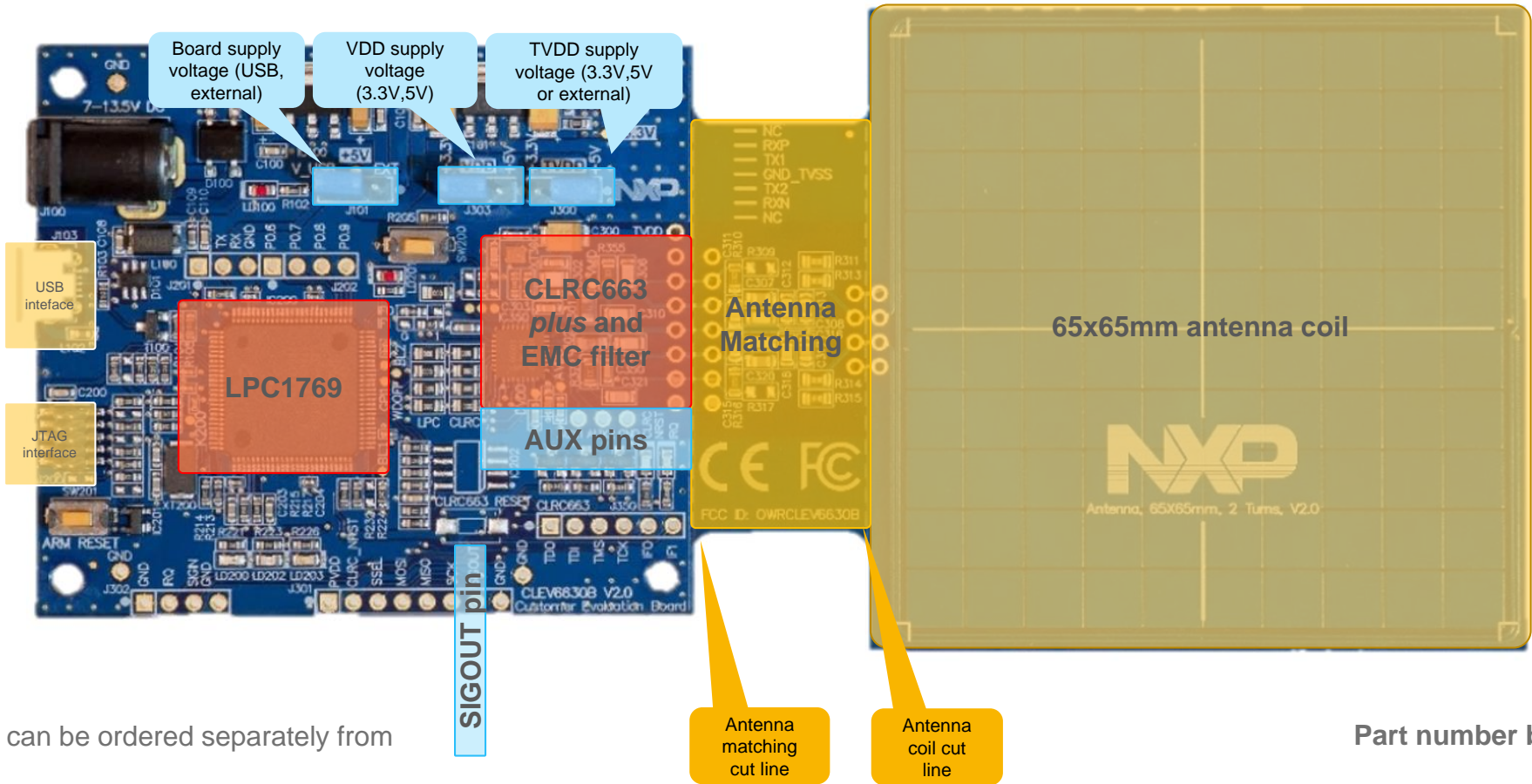
- Development kit with integrated NXP LPC1769 MCU
- Straightforward antenna design with NFC Cockpit tool
- Different antenna PCBs for easy antenna matching
- Easy application development with NFC Reader Library
- CE / FCC certified CLEV6630B board

For additional information please visit: [www.nxp.com/demoboard/OM26630](http://www.nxp.com/demoboard/OM26630)

Part number complete kit: OM26630FDK  
12NC: 9353 391 51699

# CLEV6630B details

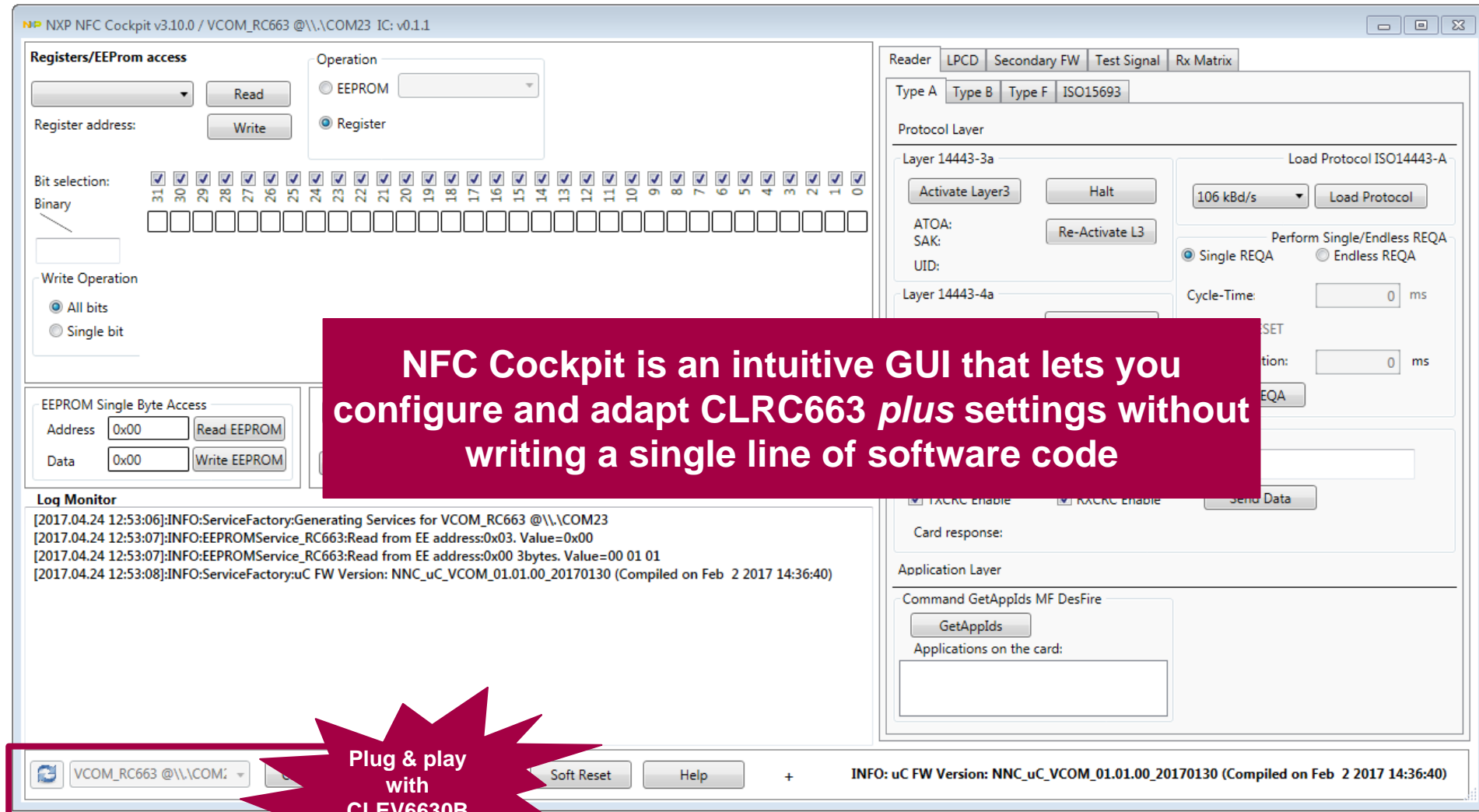
CLEV6630B  
schematics and  
layout available



\*The CLEV6630B board can be ordered separately from the OM26630FDK kit

Part number board only: CLEV6630B  
12NC: 9353 391 49699

# NFC Cockpit





# NFC Cockpit

The screenshot displays the NXP NFC Cockpit v3.10.0 interface, which is divided into several functional sections:

- Registers/EEProm access:** Located at the top left, it includes fields for "Register address", "Read", "Write", and "Operation" (EEPROM or Register). Below this is a "Bit selection" table with checkboxes for bits 31 down to 0, and a "Write Operation" section with "All bits" and "Single bit" options.
- EEPROM Single Byte Access:** A section for reading and writing EEPROM data, featuring "Address", "Data", "Read EEPROM", "Write EEPROM", and "Dump EEPROM" controls.
- RF Field Control:** Controls for "Rf Field On", "Rf Field Off", and "Rf Field Reset".
- Log Monitor:** A text area at the bottom left showing system logs, including service generation, EEPROM reads, and firmware version information.
- Protocol Layer:** The right-hand side of the interface, containing tabs for "Reader", "LPCD", "Secondary FW", "Test Signal", and "Rx Matrix". It includes sub-sections for:
  - Layer 14443-3a:** Controls for activating/halting Layer 3, ATOA, SAK, and UID.
  - Layer 14443-4a:** Controls for selecting baud rate, activating/deselecting Layer 4, and ATS.
  - Layer 14443-4: Data Exchange with PICC:** Controls for sending data, enabling TXCRC and RXCRC, and viewing card responses.

Callouts from the image highlight the following features:

- ISO/IEC14443 protocol activation:** Points to the "Type A", "Type B", "Type F", and "ISO15693" tabs in the Protocol Layer.
- Card type operations for the different protocols:** Points to the "Load Protocol ISO14443-A" button.
- Bit rate selection:** Points to the "106 kBd/s" dropdown menu.
- Execute single or endless REQ:** Points to the "Single REQA" and "Endless REQA" radio buttons.
- ISO/IEC14443 transparent data exchange:** Points to the "Data to be send:" field and "Send Data" button.
- Direct register access (including bit descriptions):** Points to the "Bit selection" table.
- Direct EEPROM Read & Write:** Points to the "Read EEPROM" and "Write EEPROM" buttons.
- Log info & history:** Points to the "Log Monitor" text area.

# NFC Cockpit - LPCD

The screenshot shows the NXP NFC Cockpit v3.10.0 interface. The title bar reads "NXP NFC Cockpit v3.10.0 / VCOM\_RC663 @\\.\COM23 IC: v0.1.1". The interface is divided into several sections:

- Registers/EEProm access:** Includes a dropdown for "Operation" (EEPROM or Register), "Read" and "Write" buttons, a "Register address" field, and a "Bit selection" section with checkboxes for bits 31 down to 0. Below this is a "Write Operation" section with "All bits" and "Single bit" radio buttons.
- EEPROM Single Byte Access:** Includes "Address" and "Data" fields (both set to 0x00), "Read EEPROM", and "Write EEPROM" buttons.
- RF Field Control:** Includes "Load EEPROM", "Dump EEPROM", and "RF Field On/Off/Reset" buttons.
- Log Monitor:** Displays a log of system events with timestamps.
- LPCD Configuration:** A tabbed section with sub-tabs for "Reader", "LPCD", "Secondary FW", "Test Signal", and "Rx Matrix".
  - Timer Configuration:** Includes "On/Off Timers", "RF Off Time" (8 ms), "RF On Time" (10 us), and a "Write T3/T4" button.
  - Timers Register Info:** A table showing register values for T4ReloadHi, T3ReloadHi, T4ReloadLo, T3ReloadLo, T4Clk, and T3Clk.
  - Current I and Q values:** Displays "LpcdResult\_I" and "LpcdResult\_Q" with a "Calibrate and Read I/Q" button.
  - Lpcd Options Configuration:** Includes checkboxes for "LPCD\_CHARGEUMP", "LPCD\_FILTER", "LPCD\_I\_UNSTABLE (RO)", and "LPCD\_Q\_UNSTABLE (RO)". It also has "Lpcd Options Register" (0x00), "Lpcd Detection Options" (High Detect Range Option, Manual Selection Option), and "Detection Thresholds" (+0 and -0, +1 and -1, +2 and -2).
  - Sensitivity Configuration:** Includes "Masked Threshold Values" (Lpcd IMax, Lpcd IMin, Lpcd QMax, Lpcd QMin) and "Actual Register Values" (LPCD\_IMIN, LPCD\_QMAX, LPCD\_QMIN).
  - Lpcd Operation:** Includes "Single Lpcd", "Endless Lpcd", and "Stop Lpcd" buttons, along with a "WakeUps" counter set to 0.

Callouts from the image:

- "Define LPCD RF ON and standby time" points to the "RF On Time" field in the Timer Configuration section.
- "LPCD calibration values" points to the "Current I and Q values" section.
- "LPCD options selection (Charge Pump & LPCD filter)" points to the "Lpcd Options Configuration" section.
- "LPCD manual sensitivity configuration (optional)" points to the "Sensitivity Configuration" section.
- "Execute single or endless LPCD loop" points to the "Lpcd Operation" section.

# NFC Cockpit – Secondary FW

NXP NFC Cockpit v3.10.0 / VCOM\_RC663 @\\.\COM23 IC: v0.1.1

**Registers/EEPROM access**

Operation: ☐ EEPROM ☒ Register

Register address:  Read Write

Bit selection: ☒ 31 ☒ 30 ☒ 29 ☒ 28 ☒ 27 ☒ 26 ☒ 25 ☒ 24 ☒ 23 ☒ 22 ☒ 21 ☒ 20 ☒ 19 ☒ 18 ☒ 17 ☒ 16 ☒ 15 ☒ 14 ☒ 13 ☒ 12 ☒ 11 ☒ 10 ☒ 9 ☒ 8 ☒ 7 ☒ 6 ☒ 5 ☒ 4 ☒ 3 ☒ 2 ☒ 1 ☒ 0

Binary:

Write Operation: ☒ All bits ☐ Single bit

**EEPROM Single Byte Access**

Address:  0x00 Read EEPROM

Data:  0x00 Write EEPROM

**RF Field Control**

Load EEPROM Dump EEPROM

**Log Monitor**

[2017.04.26 09:28:37]:INFO:ServiceFactory:Generating Services for VCOM\_RC663 @\\.\COM23  
[2017.04.26 09:28:38]:INFO:EEPROMService\_RC663:Read from EE address:0x03. Value=0x00  
[2017.04.26 09:28:38]:INFO:EEPROMService\_RC663:Read from EE address:0x00 3bytes. Value=00 01 01  
[2017.04.26 09:28:38]:INFO:ServiceFactory:uC FW Version: NNC\_uC\_VCOM\_01.01.00\_20170130 (Compiled on Feb 2 2017 14:36:40)

**Secondary FW**

Secondary Firmware Task List

EMVCo Loop Back  
Transsend A  
Transsend B

Load and execute LPC code, which are provided in the NFC Cockpit installation directory

VCOM\_RC663 @\\.\COM:    - Status: Read Register LPCD\_IMIN\_REG@0x41. Value=0x88

# NFC Cockpit – Test signals

The screenshot displays the NXP NFC Cockpit v3.10.0 software interface, which is used for configuring and testing NFC devices. The interface is divided into several sections:

- Registers/EEProm access:** This section allows users to read or write data to the device's registers or EEPROM. It includes a dropdown for the operation (EEPROM or Register), a text field for the register address, and buttons for Read and Write. Below this is a bit selection table with checkboxes for bits 31 down to 0.
- Write Operation:** This section allows users to select the write operation (All bits or Single bit).
- EEPROM Single Byte Access:** This section allows users to read or write a single byte of data to the EEPROM. It includes text fields for the address and data, and buttons for Read EEPROM and Write EEPROM.
- RF Field Control:** This section allows users to control the RF field (Rf Field On, Rf Field Off, Rf Field Reset).
- Log Monitor:** This section displays a log of events, including service factory information, EEPROM reads, and firmware version details.
- Test Signal:** This section is highlighted with a blue box and contains controls for AUX1, AUX2, and SIGOUT. It includes radio buttons for Analog and Digital, and dropdown menus for selecting the test signal type (e.g., ADC - Q, ADC - I, Tx Envelope, Tx Active Signal, S3C Generic, RX Envelope, RX Active, RX Bit).

Callouts from the text 'Analog test signals' point to the 'Analog' radio buttons in the AUX1 and AUX2 sections. A callout from 'Digital test signals' points to the 'Digital' radio button in the SIGOUT section. A callout from 'SIGOUT pin' points to the 'SIGOUT' pin on the physical board diagram. A callout from 'AUX pins' points to the 'AUX1' and 'AUX2' pins on the physical board diagram.

The physical board diagram shows the NXP NFC Cockpit v3.10.0 hardware. The board is a blue PCB with various components, including the NXP NFC chip, capacitors, and resistors. The board is labeled 'CLEV6630B V2.0 Customer Evaluation Board'. The callouts indicate the locations of the SIGOUT and AUX pins on the board.

# NFC Cockpit – Rx matrix

The screenshot shows the NXP NFC Cockpit v3.10.0 interface. The 'Rx Matrix' tab is active, displaying a 'Load And Parse XML' button, a 'Start RxMatrix' button, and a 'Stop RxMatrix' button. A table shows 'DATA SENT' (26), 'EXP DATA READ' (44 03), 'SHORT FRAME' (Yes), 'INVERTED MASK BYTES' (00 00), 'TX CRC' (No), and 'RX CRC' (No). A 'View Output' button is at the bottom right. A status bar at the bottom indicates 'INFO: Sleeping for few seconds for XML to Parse'.

Annotations include:

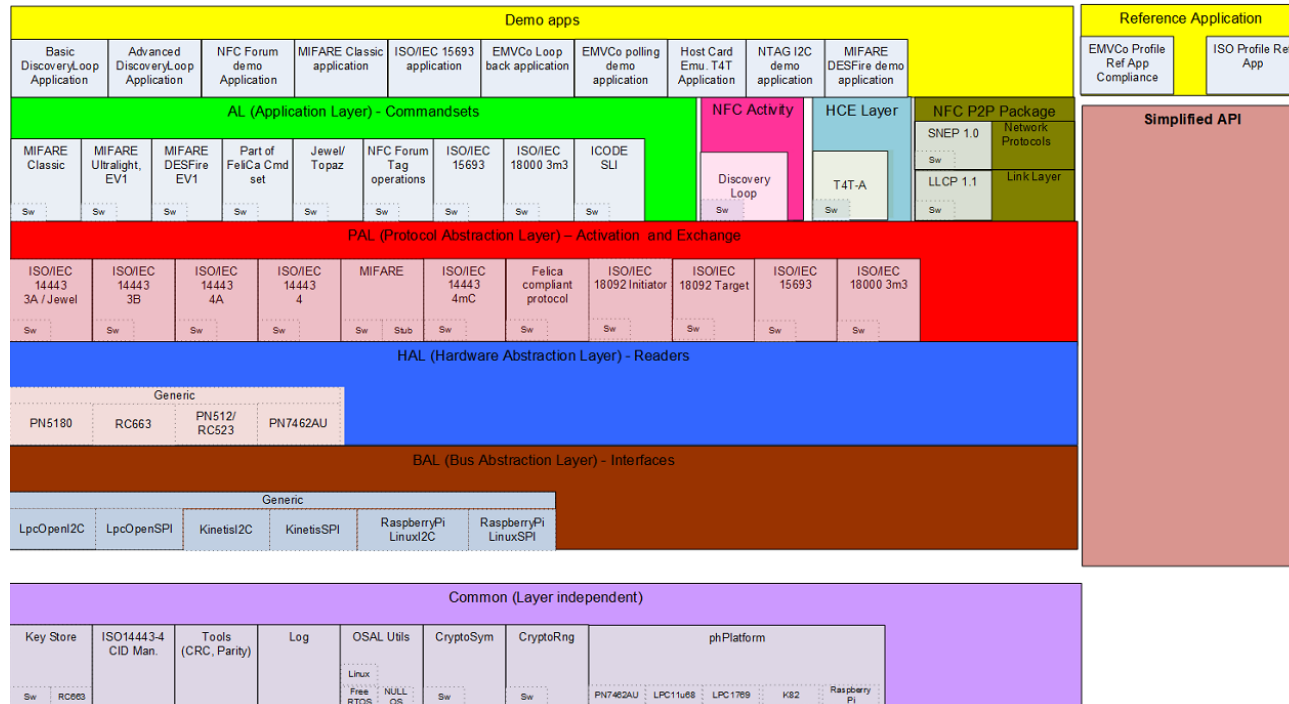
- Define an XML-based script executing a permutation of different Rx register settings**: Points to a file explorer window showing a list of XML files (e.g., type\_a\_two\_reg\_by\_name.xml, type\_a\_two\_reg\_range.xml, type\_a\_two\_reg\_sequence.xml, type\_b\_tuning.xml, type\_b\_two\_reg\_by\_name.xml, type\_b\_two\_reg\_range.xml, type\_b\_two\_reg\_sequence.xml, type\_f\_two\_reg\_by\_name.xml, type\_f\_two\_reg\_range.xml, type\_f\_two\_reg\_sequence.xml).
- Start the matrix test**: Points to the 'Load And Parse XML' button.
- Individual register settings during matrix test**: Points to the 'Start RxMatrix' button.
- Watch progress and check the results**: Points to the 'View Output' button.

The interface also includes a 'Registers/EEPROM access' section with 'Read' and 'Write' buttons, a 'Register address' field, and a 'Bit selection' section with checkboxes for bits 31 down to 0.

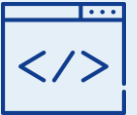
Allows to easily optimize RX settings without requiring extensive test signal debugging know how

# NFC Reader Library

## NFC Reader Library



## Software examples



- Example 1: BasicDiscoveryLoop
- Example 2: AdvancedDiscoveryLoop
- Example 3: NFCForum
- Example 4: MIFARE Classic
- Example 5: ISO15693
- Example 6: EMVCo Loopback
- Example 7: EMVCo Polling
- Example 8: HCE T4T
- Example 9: NTAG I2C
- Example 10: SimplifiedAPI\_EMVCo
- Example 11: SimplifiedAPI\_ISO

For additional information and source code, please visit: [www.nxp.com/pages/:NFC-READER-LIBRARY](http://www.nxp.com/pages/:NFC-READER-LIBRARY)

The NFC Reader Library is everything you need to create your own software stack and application for a contactless reader

# Documentation



**High-performance multi-protocol NFC frontend CLRC663 and CLRC663 *plus***  
Product data sheet



**AN11873 – CLRC663 *plus* Low Power Card Detection**  
Describes the principle of the Low Power Card Detection (LPCD), how to use it and how to optimize the related settings.



**AN11022 – CLRC663 evaluation board quick start guide**  
Describes the CLEV6630B board and how to use it together with the NFC Cockpit.

Updated

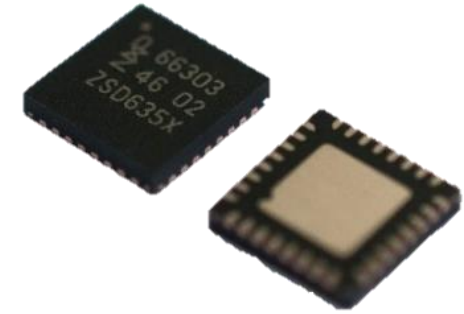


**AN11019 – CLRC663, MFRC631, SLRC610 Antenna design guide**  
Describes the principles of antenna tuning for CLRC663 product family

Updated



# Ordering details



Part number	12NC		MOQ
CLRC66303HN reel	9353 062 08518	CLRC663 <i>plus</i> ICs on reel	6000
CLRC66303HN single tray	9353 062 08551	CLRC663 <i>plus</i> ICs on multiple trays	490
OM26630FDK	9353 391 51699	CLRC663 <i>plus</i> frontend development kit containing a CLEV6630B development board and - an 30*50mm <sup>2</sup> antenna with matching components and 3 PCBs for individual antenna matching - NTAG216F and MIFARE DESFire EV2 sample cards and 10 CLRC663 <i>plus</i> samples	1
CLEV6630B	9353 391 49699	CLRC663 <i>plus</i> frontend development board with 65*65mm <sup>2</sup> antenna	1

Product samples and development boards can be ordered directly from the websites via [buy direct](#).



**Software development** in Android and iOS

**Embedded software** for MCUs

**JCOP, Java Card** operating Systems

**Hardware design and development**

Digital, analog, sensor acquisition, power management

**Wireless communications** WiFi, ZigBee, Bluetooth, BLE

**Contactless antenna** RF design, evaluation and testing

**MIFARE** applications

End-to-end systems, readers and card-related designs

**EMVco** applications

Readers, cards, design for test compliancy (including PCI)

**Secure Element management**

GlobalPlatform compliant backend solutions

**Secure services provisioning** OTA, TSM services



We help companies leverage the mobile  
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